REV 1.7

Technical Description

Fastrax IT03-02 OEM GPS Receiver

This document describes the electrical and main functionality of the Fastrax IT03-02 hardware.

April 23, 2010

Fastrax Ltd.

www.fastraxgps.com

Fastrax

TRADEMARKS

Fastrax is a registered trademark of Fastrax Ltd.

All other trademarks are trademarks or registered trademarks of their respective holders.

COPYRIGHT

DISCLAIMER

This document is compiled and kept up-to-date as conscientiously as possible. Fastrax Ltd. cannot, however, guarantee that the data are free of errors, accurate or complete and, therefore, assumes no liability for loss or damage of any kind incurred directly or indirectly through the use of this document. The information in this document is subject to change without notice and describes only generally the product defined in the introduction of this documentation. Fastrax products are not authorized for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. Fastrax will not warrant the use of its devices in such applications.

CHANGE LOG

Rev.	Notes	Date
1.0	Initial revision	2004-12-07
1.1	Pages 9, 14, 21, 23, 26	2005-01-12
1.2	Tables 3, 4, 9 and chapters 6.5.4, 7.5	2005-02-24
1.3	Corrected protocol and serial port configuration	2005-11-04
1.4	Added Application Board documentation, corrected UI C (valid fix) indicator polarity	2006-01-10
1.5	Name change to IT03-02, corrected Pull-up and Pull-down resistor values, added chapter on Wakeup control input	2009-05-27
1.6	Added disclaimer, packaging and marking codes, updated application circuit diagram	2010-02-09
1.7	Added notes and spec on ESD, ultrasonic sensitivity and RoHS; updated disclaimer; added chapter 5.2 Assembly	2010-04-23

CONTENTS

COMPLEMENTARY READING

The following reference documents are complementary reading for this document:

Ref. #	File name	Document name
1	PRO_NMEA.html	NMEA Protocol, Fastrax Oy
2	PRO_ITALK.html	iTalk Protocol Specification, Fastrax Oy
3	uN8130T_UM.pdf	uN8130 User's manual

1 GENERAL DESCRIPTION

1.1 General

Fastrax IT03-02 module is intended for a replacement of the iTrax02 module. The internal hardware of the module is identical to Fastrax IT03 GPS receiver but the physical layout is identical to iTrax02. An existing iTrax02 based design will also work with IT03-02 and a smooth transition from iSuite02 to iSuite03 environment is provided.

IT03-02 performance is identical to IT03. This means better tracking and navigation sensitivity and smaller power consumption compared to iTrax02.

The IT03-02 module interfaces to customer's application via a versatile I/O and it supports several external devices including timers, pulse measurement inputs and the MMC bus. All the peripherals have a shared functionality with General Purpose Input/Output (GPIO) interface.

The antenna input supports passive and active antennas. The active antenna bias voltage is supplied through an antenna DC bias input pin. The biasing circuit is compatible with iTrax02.

This document describes the electrical connectivity and main functionality of the IT03-02 hardware.

1.2 Block diagram

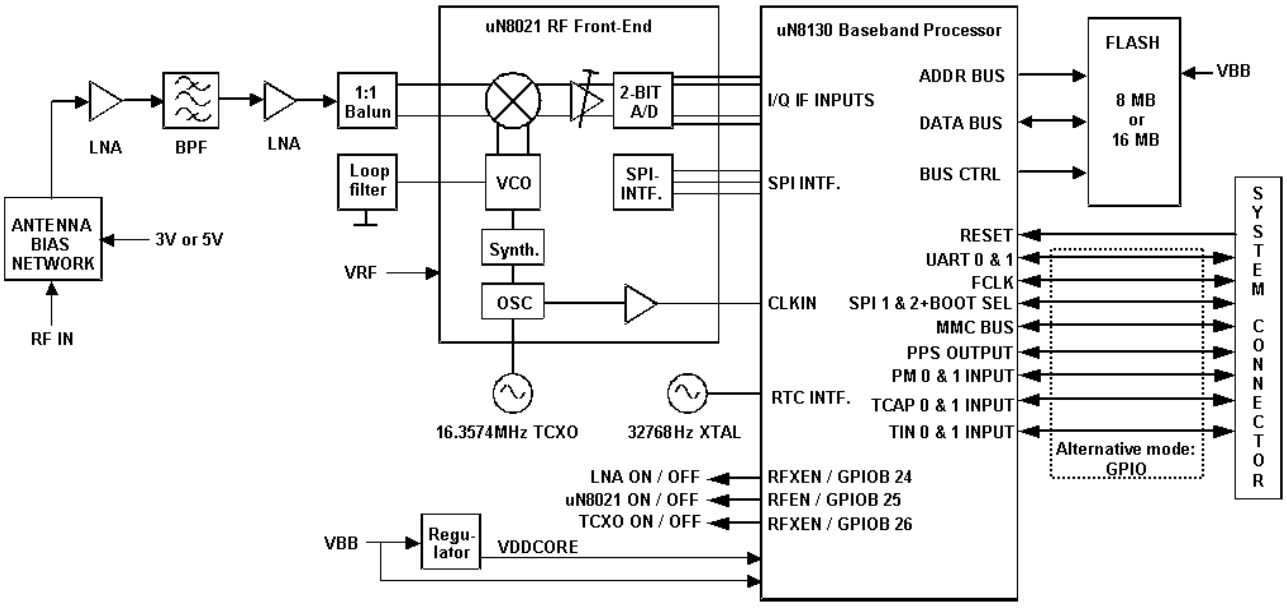


Figure 1 Block diagram

1.3 Frequency Plan

Clock frequencies generated internally at the IT03-02 receiver:

- 32768 Hz Real Time Clock (RTC)
- 16.3574 MHz Master Clock
- 1574.40 MHz Local Oscillator of the RF down-converter

2 SPECIFICATIONS

2.1 General

Table 1 General specifications

Receiver	GPS L1 C/A-code, SPS
Channels	12
Update rate	< 5 Hz, 1 Hz (default).
Supply voltage range, VRF	+2.7V…+3.3 V, low ripple 2mV RMS, max.
Supply voltage range, VBB	+2.7V…+3.3 V
Power consumption	100 mW typical (without antenna bias)
Antenna net gain range	0…+32 dB
Antenna bias voltage	Externally supplied through V_ANTENNA pin, voltage range 0…+5V.
Antenna bias current	Must be externally limited by V_ANTENNA supply to 150 mA max.
Operating and storage temperature	-40ºC…+85ºC
Serial port configuration (default)	Port 0: iTalk Port 1: NMEA
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed	600, 1200, 2400, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800, 921600 baud. NMEA: 4800(default), iTalk: 115200(default).
I/O signal levels	CMOS compatible: low state 0.0…0.3xVBB; high state 0.7…1.0xVBB
I/O sink/source current per contact	+/- 2 mA max.
PPS modes *(not yet implemented)*	Off, Survey, Static, Roving (default)
Accessory I/O (shared functionality with GPIO)	2xCapture Timers, 2xPulse Measurement Inputs, 1xSPI-bus, MMC bus

2.2 Absolute maximum ratings

Table 2 General specifications

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation		500	mW
Supply voltage, VBB	-0.3	+3.6	V
Supply voltage, VRF	-0.3	+3.6	V
Current on any I/O pin except antenna input	-30	+30	mA
Current output on antenna input	0	+150	mA
Input voltage on any input connection	-0.3	VBB + 0.3	V
ESD voltage (RFIN, Machine Model)		±160	V
RFIN input power	-	+15	dBm

3 OPERATION

3.1 Operating modes

After power-up IT03-02 boots from the internal Flash memory for normal operation. Modes of operation:

- Navigation/Idle mode
- Sleep mode
- Programming mode

3.2 Navigation/Idle mode

The IT03-02 receiver enters Navigation mode after the power up. By default it will start navigation automatically after power-up or reset in Auto Start mode. Auto Start mode means that all available aiding information will be used.

The module operates as long as the power supply is connected.

Idle mode means that the navigation is stopped but the processor still remains active. Navigation / Idle mode is also referred as ***Normal*** mode.

The standard firmware supports versatile configuration of various operating configurations, e.g. Logging position data etc., for further details see *ref 1* and *ref 2*.

The navigation can be stopped by sending a proper NMEA or iTALK message, see also *ref 1* and *ref 2*.

3.3 Navigation/Idle mode

The Sleep mode means low power operation during which no other activity other that the internal real time clock (RTC) is present. The module enters Sleep mode via a special control message (*ref #1*) or by the On/Off Control input.

The exit from the Sleep mode to the Normal mode happens in the following situations:

- an elapsed time
- an RS-232 break signal or a dummy input character to selected serial port (the low input state should exceed 20ms)
- an interrupt from the On/Off Control input (low-to-high transition)
- an interrupt from the Wake-up input (low/high or high/low transition).

Since the internal RTC keeps the GPS time estimate, the module performs the fastest possible navigation start depending on the availability of valid satellite/position data.

3.4 Programming mode

The module enters Programming mode by two methods: HW-booting or upgrading the firmware on-the-fly by a dedicated NMEA or iTalk command, see *ref 1*.

The on-the-fly upgrading requires only the serial Port 0. The downloading will start by sending a special serial port command, after which the utility running on the host will send the new firmware to the processor.

HW-booting is utilized by keeping the Boot Select (pin 17, SPI2XCS3/GPIOB22) at logic low during power up or system reset. Now the GPS module boots from the serial data Port 0, sends hex 55 (U) string at 9600 baud and waits for the boot loader commands from the host (an application running on the host). This mode is required when there is no existing firmware stored into the internal Flash memory.

It is recommended to support hardware based re-programming (HW-booting) in an IT03-02 application. This is done by adding Boot Select and XRESET control inputs into the design. See the reference design.

4 CONNECTIVITY

4.1 System connector

A 40-pin system connector is located on the bottom side of the GPS module. It is a 2x20 pin, 0.50mm pitch board-to-board connector (manufacturer AMP, product code 4-353515-0).

The suitable mating connector is AMP 4-353512-0 (see Appendix); samples are available from Fastrax Ltd.

The logic signals at the system connector are connected to uN8130 GPS processor IC through 220 ohm series resistors.

In the following table shows the I/O functionality with default firmware for each signal of the system connector. Unlike with iTrax02, many IT03-02 pins have two different modes, a general purpose I/O mode and a custom purpose mode. The selection of the pin mode is done with the IT03-02 firmware.

Table 3 System connector

Pin	Pin mode	Dir.	GPIO mode (1)	Default function description	iTRAX02 con.
1	GPIO A4, FCLK	OUT	PUSH-PULL	Debug LED 1	GPIO0
2	GPIO B10, SPI1XCS0	IN	PULL-UP	*GPIO reserved for future use. Do not connect.*	GPIO1
3	GPIO B20, SPI2XCS1	OUT	PUSH-PULL	User interface LED C (Valid fix ind.)	GPIO2
4	GPIO A8, TIN0	OUT	PUSH-PULL	Debug LED 4	GPIO3
5	GPIO A9, TCAP0	OUT	PUSH-PULL	Debug LED 5	GPIO4
6	GPIO A10, TIN1	OUT	PUSH-PULL	Debug LED 6	GPIO5
7	GPIO A11, TCAP1	OUT	PUSH-PULL	Debug LED 7	GPIO6
8	GPIO A12, MCCCLK	OUT	PUSH-PULL	Debug LED 8	GPIO7
9	GPIO A13, MMCCMD	OUT	PUSH-PULL	User interface LED B	GPIO8
10	GPIO A14, MMCDAT	OUT	PUSH-PULL	User interface LED A	GPIO9
11	GPIO B13, SPI1CLK	IN	PULL-DOWN	*No default function*	GPIO10
12	GPIO B15, SPI1SDI	IN	PULL-DOWN	External wake up	GPIO11
13	GPIO B14, SPI1SDO	IN	PULL-DOWN	*No default function*	GPIO12
14	RFXEN	OUT	-	LNA control (0:LNA ON, 1:LNA OFF)	GPIO13
15	GPIO B0, KBDOUT0	IN	PULL-UP	*No default function, not a Boot select.*	GPIO14
16	GND	GROUND	-	Power and signal ground	GND
17	GPIO B22, SPI2XCS3	I	PULL-UP	Boot mode select, internal 15k pull-up	GPIO15
18	GND	GROUND	-	Power and signal ground	GND
19	GPIO A5, PM0	OUT	PUSH-PULL	Debug LED 2	PM0
20	GPIO A6, PM1	OUT	PUSH-PULL	Debug LED 3	PM1
21	GPIO B18, SPI2SDI	IN	PULL-UP	On / Off control input	SPI_SDI
22	GPIO B17, SPI2SDO	IN	PULL-DOWN	*No default function*	SPI_SDO
23	GPIO B16, SPI2CLK	IN	PULL-DOWN	*No default function*	SPI_SCK
24	GPIO B19, SPI2XCS0	IN	PULL-DOWN	*No default function*	SPI_XCS0
25	RXD0, GPIO A0	IN	-	UART port 0, receive data	RXD0
26	TXD0, GPIO A1	OUT	-	UART port 0, transmit data	TXD0
27	RXD1, GPIO A2	IN	-	UART port 1, receive data	RXD1
28	TXD1, GPIO A3	OUT	-	UART port 1, transmit data	TXD1
29	VBB	IN	-	2.7V to 3.3V regulated DC power supply	VBB
30	PPS, GPIO A7	OUT	-	PPS signal output	PPS
31	XRESET	IN	-	External Reset, Active Low, internal pull-up	XRESET
32	GND	GROUND	-	Power and signal ground	GND
33	VRF	IN	-	2.7V to 3.3V regulated DC power supply	VRF
34	GND	GROUND	-	Power and signal ground	GND
35	GND	GROUND	-	Power and signal ground	GND
36	GND	GROUND	-	Power and signal ground	GND
37	RF	RF IN	-	RF input, 50 ohm & antenna bias ouput	RF
38	V_ANTENNA	IN	-	Antenna bias DC power supply	V_ANTENNA
39	GND	GROUND	-	Power and signal ground	GND
40	GND	GROUND	-	Power and signal ground	GND

Note (1): GPIO Input has either Pull-down resistor 9kohm (typ.) or Pull-up resistor 18k (typ.)

4.2 Notes for iTrax02 replacement

There are few differences between IT03-02 and iTrax02. These are:

- Pin 15 in IT03-02 connector does not support an SPI boot. In iTrax02 this pin was GPIO14 and it was also used for boot device selection. In IT03-02 the logic state of pin 15 during the boot-up is irrelevant in default firmware configuration.

- There is no more need for an external power-on-reset (POR) delay. However, the XRESET low assertion should be greater than 0.5 ms. If XRESET signaling is not required in the target system, the XRESET pin can be left floating. However, it is

recommended to connect XRESET in the design, so the HW based re-programming can be done. (Also Boot Select is needed for HW based re-programming.)

- IT03-02 has an internal watchdog, which will reset the module software internally, if triggered.
- With standard firmware the signaling related to indicator outputs, i.e. Debug LEDs and User Interface LEDs, differ from iTrax02 signaling.
- There are more peripherals and GPIO input/output available through custom software.
- VBB supply input has internal low ESR (0.01 ohm) ceramic 1uF by-pass capacitor. Ensure that the power supply is specified and stable with low ESR (0.01 ohm) output load capacitors.

5 MECHANICAL DIMENSIONS

5.1 Mechanical dimensions and contact numbering

Module size is 25.9mm (width) x 25.9mm (length) x 4.7mm (height). General tolerance is ±0.3mm.

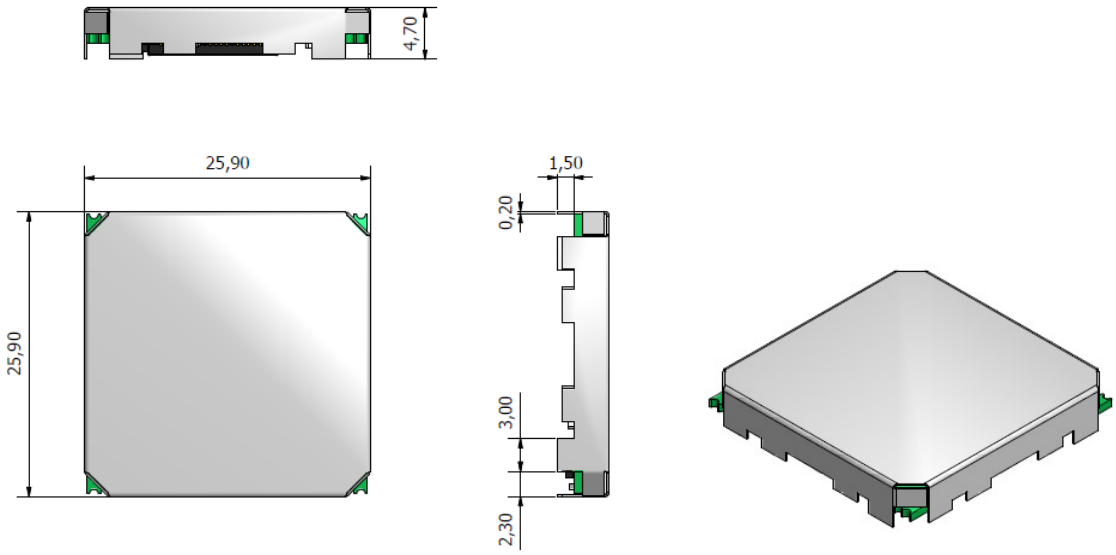


Figure 2 Dimensions

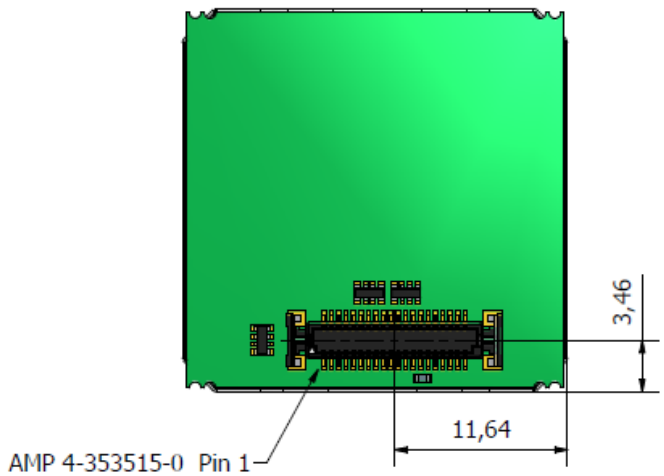


Figure 3 Contact numbering and connector location, bottom view.

5.2 Assembly

Module is intended for hand assembly on the mating interface connector and hand soldering the shield on four GND pads to the motherboard.

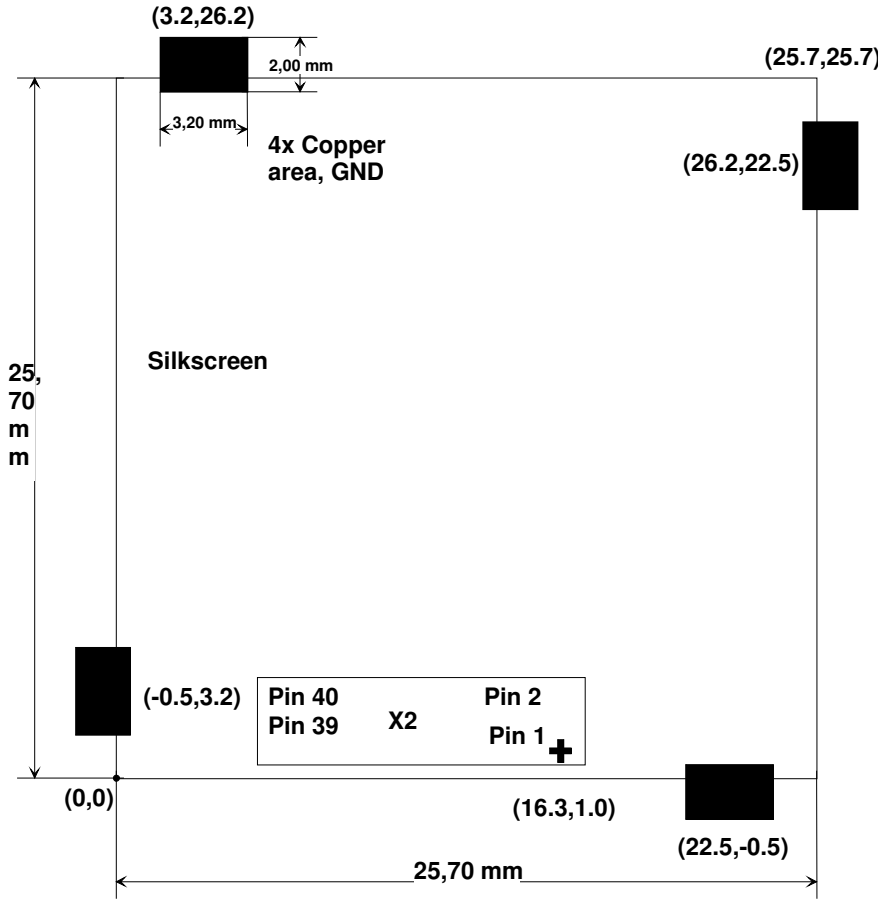


Figure 4 Pad dimensions for GND soldering pads, top view. Solder GND pads to the shield of the IT03-02 module.

A solid ground plane should be used below the IT03-02 module on the customer's PCB to reduce the LO-leakage on 1574.40 MHz. This is essential when the GPS antenna is close (<0.2m) to the module, otherwise the receiving performance may be degraded.

Note that module is Electrostatic Sensitive Device (ESD). Rated voltage is 160V max (Machine Model) at antenna input RFIN signal.

NOTE

Note that module is Electrostatic Sensitive Device (ESD), rating 160V max (Machine Model) at RFIN.

Avoid also ultrasonic exposure due to internal crystal and SAW components.

The module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). For details contact Fastrax support.

5.3 Packaging

Modules are packed in a tray; dimensions are 314x515x8mm. One tray contains up to 100 pcs and one shipping box (320x550x100mm) contains up to 10 trays, i.e. 1000 pcs.

5.4 Marking

Module marking includes type and batch codes and serial number.

Type code is e.g. **IT3216-341D-STD-3279** (may vary)**,** where

- **IT3216** is IT03-02 product code with internal 16 Mbit flash memory
- **341D** is SDK revision 3.4.1 and **D** is incremental firmware release revision (may vary)
- **STD** is firmware configuration code (may vary)
- **3279** is BOM (Bill-of-Materials) revision code (may vary)

Batch code is e.g.**190205** (may vary)**,** where

- **1** is factory code
- **9** is last digit of the year (e.g. 200**9**)
- **02** is month (e.g. February)
- **05** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, julian date code and incremental number.

6 ELECTRICAL SPECIFICATIONS

6.1 Power supply

The IT03-02 module requires two separate power supplies: VRF for the RF parts and VBB for digital parts and I/O bus. Note that VBB supply input contains internal ceramic 1uF low ESR (0.01ohm) by-pass capacitor. Use a power supply that is specified for low ESR (<0.01ohm) output capacitor loads. VBB and VRF should be powered up at the same time within a few ms.

The VBB supply may be shared with any available supply that meets the specified voltage range. A typical current is 12 mA in Normal (Navigation) mode but it may peak up to 40 mA for short durations. The VBB supply voltage ripple should be below 40mV (RMS).

NOTE

VBB power supply should be compatible with low ESR (<0.01ohm) ceramic capacitors.

VRF must be linearly regulated having a low ripple 2mV (RMS) max. The typical current drain is 24 mA in Normal (Navigation) mode.

NOTE

VRF supply voltage should have a low ripple 2mV(RMS) max.

6.2 Reset

The system reset input (pin 31, XRESET), is an active low asynchronous reset. The processor boots after an XRESET low-to-high transition. The XRESET input contains a 100k ohm pull-up resistor, an internal open-source Power-on-Reset (POR) circuit and a Schmitt trigger in order to eliminate the effect of noise. The POR is connected in parallel with the XRESET input and it overrides XRESET during power-up.

For normal operation the XRESET input can be left unconnected. The module will independently handle the reset during power-on. However, to enable the hardware re-programming, it is advisable to connect the XRESET input for example to an open-collector or an open-source control output.

6.3 Watchdog

The processor contains a watchdog peripheral, which resets the processor if not refreshed frequently enough. Basically the watchdog is a 16-bit counter with enabling, disabling and restarting controls. The watchdog counter is clocked with the frequency of 128 Hz.

6.4 Shared functionality

All the I/O pins have a shared functionality. These pins can be programmed either to have a special function (PM, SPI, MMC etc.) or a general purpose I/O (GPIO) function.

Each signal is named according to the special functionality but also the secondary functionality is listed as Alternative GPIO in Table 3.

With the standard firmware there are dedicated GPIO connections, which are: Boot Select, UI Indicators and the control inputs. These shall be described in the following chapters.

6.5 Dedicated GPIO

6.5.1 Boot select

The boot source is defined after power up in the internal boot ROM sector by using the pin 17 (GPIOB22 / SPI2XCS3). The boot up source is processed according to Table 5.

The pin is internally pulled high to VBB with a 15kohm pull-up resistor. In addition the Boot select input requires an external pull resistor <10kohm to ensure normal operation.

The state of the Boot Select pin is determined during power up and after XRESET low-to-high transition.

Table 4 Boot select

GPIO B22, pin 17	I/O	Signal description
High state	I	External boot sector (Flash memory), in case of failure continue with UART Port 0 boot
Low state	I	UART Port 0 boot

NOTE

The Boot select input (pin 17, SPI2XCS3/ GPIOB22) requires an external <10k ohm pull-up resistor connected to VBB for normal operation.

After power up Boot select should be kept valid for at least 100 ms.

In Normal mode the Boot Select should be kept valid for at least 30us after XRESET low-to-high transition.

For firmware re-programming both XRESET and Boot select signal control by the host is suggested.

6.5.2 UI Indicators

The default firmware includes three GPIO outputs that suitable as drivers for User Interface (UI) indicators A, B and C. These outputs can be used for example to drive LEDs, which give information on the state of the receiver.

Table 5 UI Indicators

UI Indicator	Pin number	I/O	Operation: High ratio %	Signal description
A	10	O	Continuously low state	Power Off or Sleep mode
A	10	O	Short blink 20	Normal mode, Navigation stopped
A	10	O	Long blink 80	Normal mode, Navigation started
B	9	O	Continuously low state	Navigation stopped or not tracking satellites
B	9	O	Short blink 20	Tracking satellites but not enough information to calculate pseudo-ranges
B	9	O	Long blink 80	Pseudorange information available but not navigating
B	8	O	Continuously high state	Navigating, Valid fix
C	3	O	Low state	Valid fix available
C	3	O	High state	No valid fix

The UI Indicators are updated synchronously at 1 Hz rate. The high state duty cycle is either 0% (i.e. continuously logic low), 20% (Short blink), 80% (Long blink) or 100% (i.e. continuously logic high).

Pin 15 (SPI2SDO / GPIOB17) indicates when a fix is available: the pin is logic high when location fix is valid and logic low when the location fix is invalid.

Note that the valid fix indicator C (GPIOB20, pin 3) has opposite polarity when compared to standard IT03 firmware. The aim is to follow the iTrax02 fix indicator polarity. The IT03-02 Application Board rev. A has the indicator led D1 with opposite polarity, which follows the IT03 standard firmware.

6.5.3 On/Off control input

With the standard firmware the module can be commanded to Sleep mode by the On/Off control input (pin 21, SPI2SDI / GPIOB18) or by a specific command via UART. During Sleep mode only the real time clock is running and the current consumption is reduced to about 20 uA.

Note that the worst case delay from the On/Off Control high-to-low transition to achieve Sleep mode and reduced current drain is 300 ms. The standard firmware stores the last known good position (LKG) and any Log data to the internal Flash memory before entering the Sleep mode.

Table 6 On/Off control

On/Off Control, pin 21	I/O	Signal description
High state	I	Normal (navigating) mode, delay from Sleep mode 3 ms
Low state	I	Sleep mode, delay from Normal mode 300 ms max.

NOTE

With the default firmware the On/Off control input (pin 21, SPI2SDI / GPIOB18) has an internal 18k ohm pull-up resistor connected to VBB in normal mode and the signal can be left unconnected for normal operation.

In Sleep mode the pull-up is internally switched to 9k pull-down.

6.5.4 Wakeup control input

With the standard firmware the module can be wake up from sleep state by the Wake Up control input (SPI1SDI / GPIOB15, pin #12) depending on the sleep mode wakeup mask. Wake Up input is normally used only when the module has entered sleep state using the specific serial command.

Wake up interrupt is generated by a low-high-low pulse to the Wake Up control input. The pulse length should be at least 20 ms. The input has an internal 9kohm pull-down resistor and can be left unconnected for normal operation.

6.5.5 Sleep mode and I/O

During Sleep mode the system connector pins have the logic states presented in Table 9.

Table 7 I/O signal states during Sleep mode

Pin	Pin function	Dir.	GPIO mode	Description	iTRAX02 con.
1	GPIO A4	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO0
2	GPIO B10	IN	PULL-UP	GPIO input, 18k ohm pull-up resistor	GPIO1
3	GPIO B20	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO2
4	GPIO A8	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO3
5	GPIO A9	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO4
6	GPIO A10	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO5
7	GPIO A11	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO6
8	GPIO A12	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO7
9	GPIO A13	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO8
10	GPIO A14	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO9
11	GPIO B13	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO10
12	GPIO B15	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO11
13	GPIO B14	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO12
14	RFXEN	IN	-	Low state, push-pull output	GPIO13
15	GPIO B0	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	GPIO14
16	GND	GROUND	-	Power and signal ground	GND
17	GPIOB22	IN	PULL-UP	GPIO input, 18k pull-up resistor	GPIO15
18	GND	GROUND	-	Power and signal ground	GND
19	GPIO A5	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	PM0
20	GPIO A6	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	PM1
21	GPIO B18	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	SPI_SDI
22	GPIO B17	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	SPI_SDO
23	GPIO B16	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	SPI_SCK
24	GPIO B19	IN	PULL-DOWN	GPIO input, 9k ohm pull-down resistor	SPI_XCS0
25	GPIOA0	IN	PULL-UP	GPIO input, 18k ohm pull-up resistor	RXD0
26	GPIOA1	IN	PULL-UP	GPIO input, 18k ohm pull-up resistor	TXD0
27	GPIOA2	IN	PULL-UP	GPIO input, 18k ohm pull-up resistor	RXD1
28	GPIOA3	IN	PULL-UP	GPIO input, 18k ohm pull-up resistor	TXD1
29	VBB	IN	-	2.7V to 3.3V regulated DC power supply	VBB
30	GPIOA7	IN	PULL-DOWN	GPIO input, 100k ohm pull-down resistor	PPS
31	XRESET	IN	-	External Reset, Active Low, 100k pull-up	XRESET
32	GND	GROUND	-	Power and signal ground	GND
33	VRF	IN	-	2.7V to 3.3V regulated DC power supply	VRF
34	GND	GROUND	-	Power and signal ground	GND
35	GND	GROUND	-	Power and signal ground	GND
36	GND	GROUND	-	Power and signal ground	GND
37	RF	RF IN	-	RF input, 50 ohm & antenna bias ouput	RF
38	V_ANTENNA	IN	-	Antenna bias DC power supply	V_ANTENNA
39	GND	GROUND	-	Power and signal ground	GND
40	GND	GROUND	-	Power and signal ground	GND

6.6 Antenna input

The module supports both passive and active antennas. The antenna input impedance is 50 ohms. For passive antenna keep the cable loss below 1dB.

6.6.1 Active GPS antenna

The antenna input provides also a bias supply during normal navigation operation. The antenna bias voltage can be provided via externally V_ANTENNA input. The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range from +6 dB to +32 dB.

During the Sleep mode the antenna bias voltage can be switched off externally by the control of the RFXEN control output (pin 14), see the reference application circuit diagram.

The maximum tolerated antenna bias current is 150mA. It is current limited only by the external circuit supplying V_ANTENNA.

NOTE

Antenna bias current at V_ANTENNA current shall be limited externally to 150mA max to provide protection for e.g. antenna shot circuit condition.

6.7 PPS output

The PPS output (pin33) provides a pulse-per-second signal, which can be used for timing purposes. The default PPS mode is Roving, i.e. timing pulse is available after valid fix based on the current valid fix position. The operating mode, pulse length and polarity are configurable via NMEA or iTALK. Other modes are Static, Survey and Off, see *ref 1* for details.

6.8 Serial ports

The device supports UART communication via Port 0 (RXD0 & TXD0) and Port 1 (RXD1 & TXD1). With the standard firmware Port 0 is configured to iTALK by default and secondary to NMEA protocol. Port 0 is also used when the device is booting from the serial port. With the standard firmware Port 1 is configured for NMEA communication by default and secondary to iTALK.

The serial port logic levels are CMOS compatible. Thus, they are not directly compatible with RS-232 logic levels. Use an external level converter to provide RS-232 levels, when needed. Refer to ref 1 for supported data speeds.

6.9 SPI-bus

The SPI1 in reserved internally for the RF-down-converter and externally for a custom boot mode. Only the SPI2 device (master) is available for SDK users enabling SPI communication.

6.10 Capture timers

Two general-purpose timer inputs TCAP0 and TCAP1 (pins 5 and 7, respectively) are available for SDK users with a custom firmware. TMG0 and TMG1 timers have configurable pre-scalers and clock cycle counts. The clock input is selectable between three sources including TIN0 and TIN1 (pins 4 and 6, respectively) and there is a capture mode to count external events. Each timer also has a programmable delay, referenced to the internal epoch pulse (TME). This makes it possible to have a specified delay between interrupts generated by the internal TME epoch, TMG0, and TMG1. For details see *ref 2*.

6.11 Pulse measurement inputs

The two pulse measurement PM0 and PM1 inputs (pins 19 and 20, respectively) are available for SDK users with a custom firmware. PM inputs can be used to measure with great accuracy how long an input stays high or low. For details see *ref 2*.

6.12 MMC bus

The MMC bus is available for SDK users with a custom firmware. The MMC unit implements a standard 3-wire Multi Media Card serial bus interface and provides control and data register for easy usage of the bus. Both stream and block mode data transfers are supported. The CRC is calculated automatically for transmitted commands and data blocks, also received responses and data blocks are checked for correct CRC. The MMC unit has a 64-bit data buffer and is capable of stopping bus clock to prevent buffer overflow and underflow situations. For details see *ref 2*.

7 RERENCE DESIGN

The idea of the reference design is to give a guideline for the applications using the IT03-02 GPS module.

In the following two chapters the reader is exposed to design rules he should follow, when designing an IT03-02 based application. By following the rules one ends up having an optimal design with no unexpected behavior caused by the PCB itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or high speed logic.

7.1 Minimum Application Circuit Diagram

The Minimum Application circuit shown in picture 6 supports communication through the UART Port 0 with iTALK protocol (configurable to NMEA protocol). Other UART Port configuration possibility is to reserve Port 0 to service (diagnostic via iTalk and e.g. firmware update) and to use Port 1 for NMEA protocol. Required signals include also the antenna input, supply voltages for analog and digital supply inputs and a pull-up resistor for the Boot Select.

The low drop-out linear regulator (LDO) U2 supplies +2.8 V voltage to the RF and analog parts (VRF) and the digital supply (VBB) is taken directly from the main supply, which is in this case from +3.0 to +3.3 V due to the small drop-out voltage across U2. Note that VBB supply input contains internal ceramic 1uF low ESR (0.01ohm) by-pass capacitor. Use a power supply or regulator that is specified for low ESR (<0.01ohm) output capacitor loads.

The linearly regulated power supply is needed for VRF, because the maximum allowed ripple voltage for VRF is 2 mV(RMS). The external regulator U2 can be omitted, if such a supply is available that meets the specified ripple voltage. Additionally, there must be another de-coupling capacitor from VBB to the ground, i.e. C3 that is 4.7uF or larger capacitor, which can be located further away.

It is also a good practice to support hardware based re-programming of the module firmware. Due to this, one should connect Boot Select (pin 17, SPI2XCS3 / GPIOB22) in such a way, that it can be toggled to logic low during reset or power up for firmware update through serial Port 0. In normal operation Boot Select is pulled high with resistor R2. IT03-02 supports also software based “on-the-fly” programming. This does not require toggling of the Boot Select signal. However, this method is not completely protected against unexpected problems like power outage during the re-programming session. Because of this, the use of Boot Select in the design is recommended.

All the digital signals are routed away from the module through series resistors (R3… R8). In this way the local oscillator (LO) signal leakage that is present in the I/O contacts of the GPS module is suppressed. Although the LO leakage is very small at the I/O contacts of the module, it may still interfere with the GPS reception, especially when the antenna is located very near to these signal routes.

For the same reason capacitors C1 and C2 should be connected very close to the module with short traces to I/O contacts and to ground plane.

If a signal from the IT03-02 is not needed, the corresponding pin can be left open (floating). Optional Antenna Bias Voltage is provided via external switch Q1, which is controlled by the RFXEN signal from pin 14.

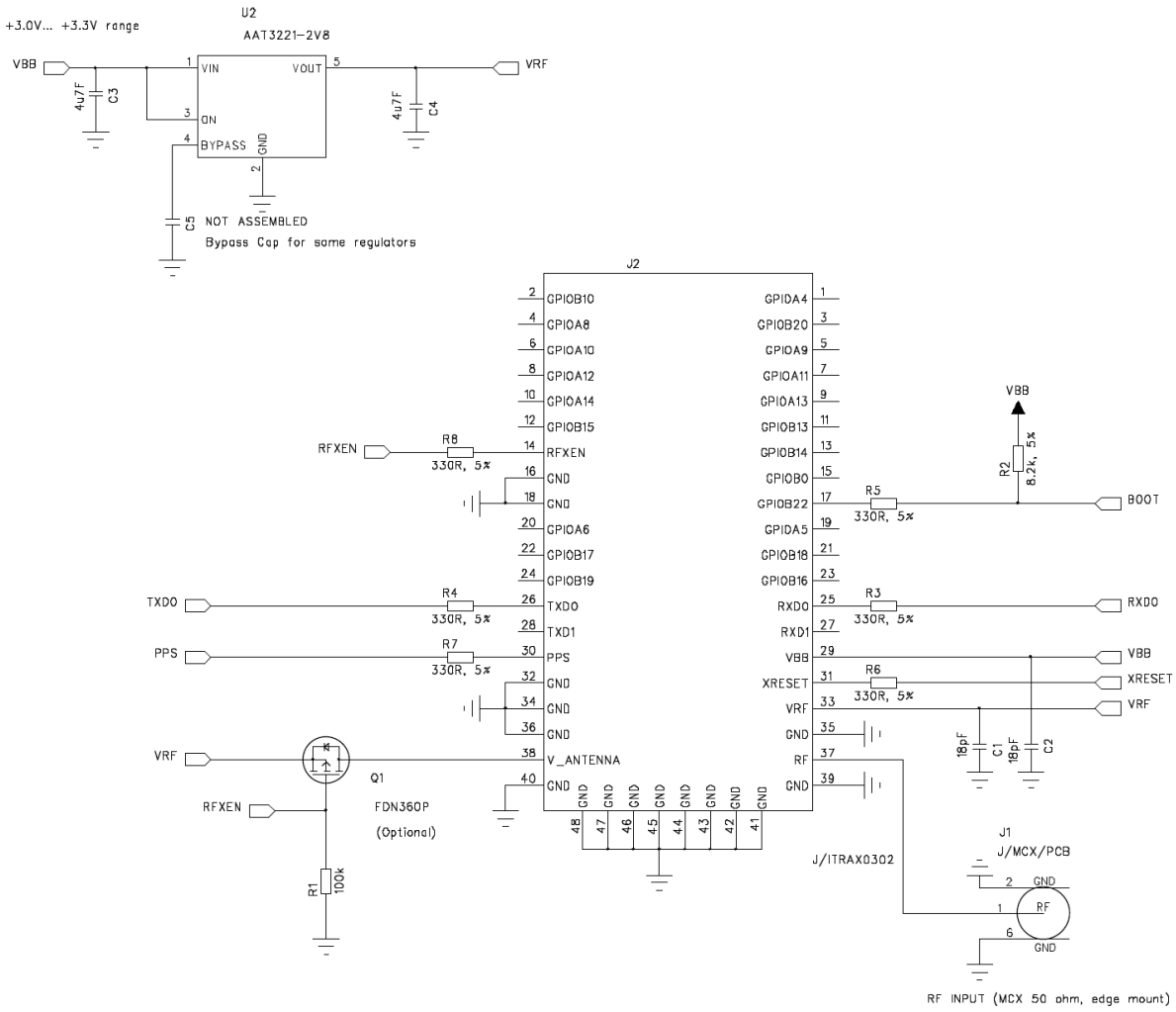


Figure 5 Minimum Application Circuit Diagram.

7.2 PCB layout suggestions

The suggested 4-layer PCB build up is presented in the following table.

Table 8 Suggested PCB build up

Layer	Description
1	Signal + Ground plane
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals directly under the module should be avoided. This area should be dedicated to ground plane, except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first layer below the IT03-02 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The by-pass capacitors or series resistors at the I/O pins should be placed very near to the IT03-02 I/O connector. In this way the risk for the local oscillator leakage is minimized. Place the GND via holes as close to the capacitor as possible.

Connect the GND soldering pads of IT03-02 to ground plane with short traces to multiple via holes, which are connected to the ground plane. Use preferably at least two VIA holes per GND pad.

The RF input should be routed clearly away from other signals. This minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With an FR-4 material the width of the trace is about two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way a solid RF ground is achieved throughout the circuit board. Several VIA holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layer, and adding copper areas to routing-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or re-flow soldering.

7.3 Antenna input pin layout

An external GPS antenna (active or passive) can be connected to IT03-02 through the RF input pin at the system connector. A 50 ohm PCB stripline is needed on the motherboard, see figure below for example layout.

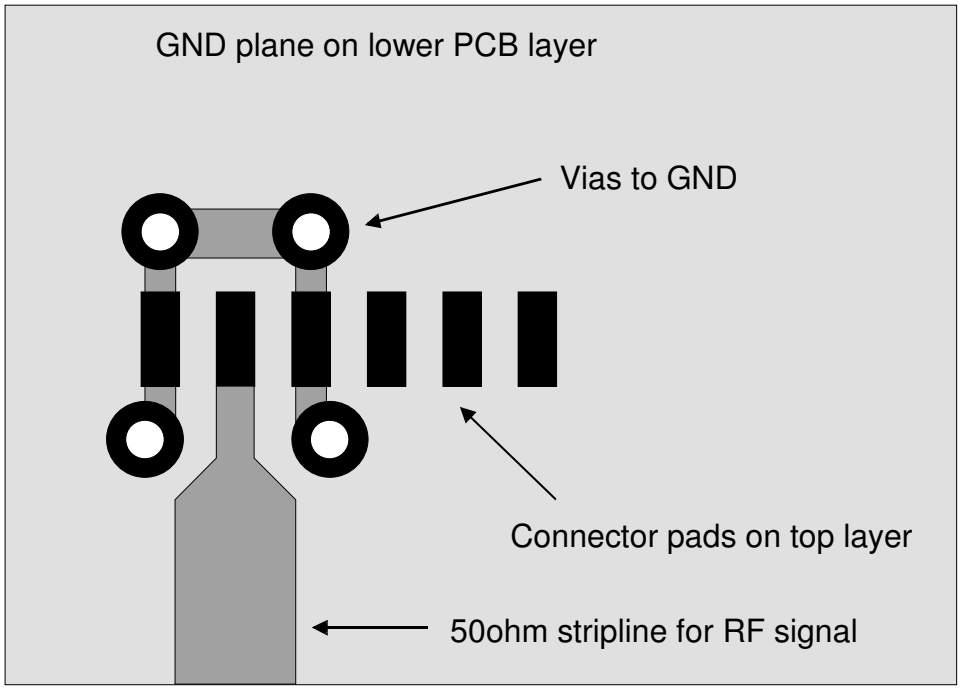


Figure 6 RF-input layout, example.

The width of the 50ohm stripline is dependent of the PCB material and thickness. On FR4 material the width [W] (at 1.6GHz) is roughly 2 times the thickness [H] of the PCB. If the PCB thickness is for example 0.8mm then the width of the stripline should be 1.6mm and so on.

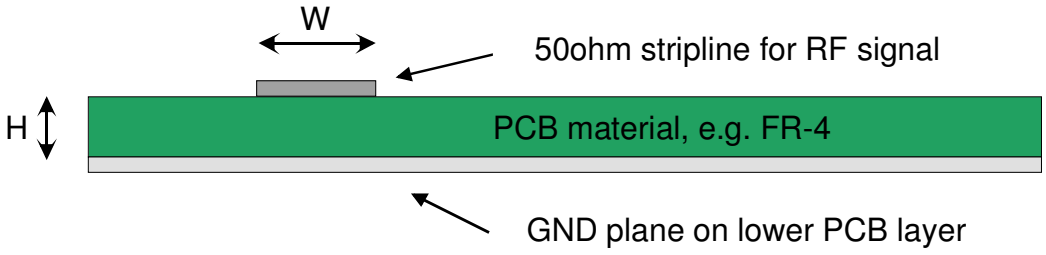


Figure 7 Stripline impedance versus PCB layer thickness.

8 APPENDIX

8.1 Mating system connector AMP 4-353512-0

0.5mm Fine Stack Receptacles, 0.5 [.020] Pitch

1.5 [.059] Stacking Height

Material and Finish:

Housing — 6T nylon, high heat resistant resin

Contacts — Phosphor bronze, plated AMP-DURAGOLD with entire contact underplated nickel

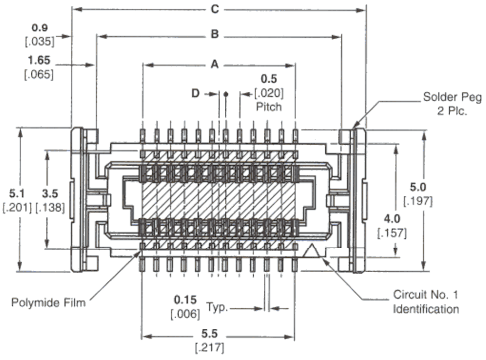
Solder Pegs — Copper alloy, plated tin-lead

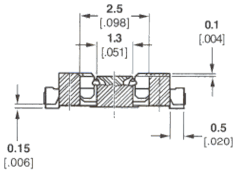
Related Product Data:

Mating Tabs — page 9

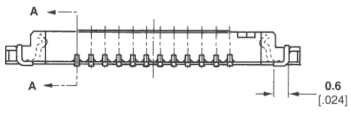
Technical Documents (Page 70):

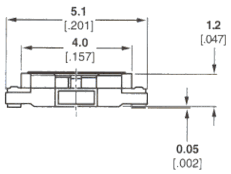
AMP Product Specification
108-5546

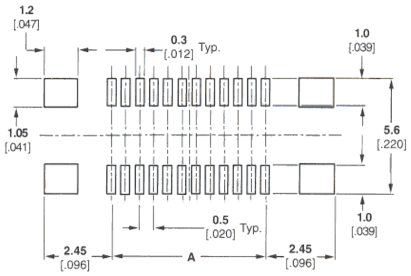




Section A - A







Recommended PC Board Layout
(PC Board Thickness = 0.6 [.024] Min.)

No. of Positions	Dimensions A	B	C	D	Keyed	Receptacle Part Numbers
20	4.5 .177	7.8 .307	9.6 .378	0.25 .010	Yes	2-353512-0
30	7.0 .276	10.3 .406	12.1 .476	0.0	Yes	3-353512-0
40	9.5 .374	12.8 .504	14.6 .575	0.25 .010	Yes	4-353512-0
50	12.0 .472	15.3 .602	17.1 .673	0.0	No	5-353159-0
60	14.5 .571	17.8 .701	19.6 .772	0.25 .010	No	6-353159-0
70	17.0 .669	20.3 .799	22.1 .870	0.0	No	7-353159-0
80	19.5 .768	22.8 .898	24.6 .969	0.25 .010	No	8-353159-0

8.2 Application board: Circuit diagram

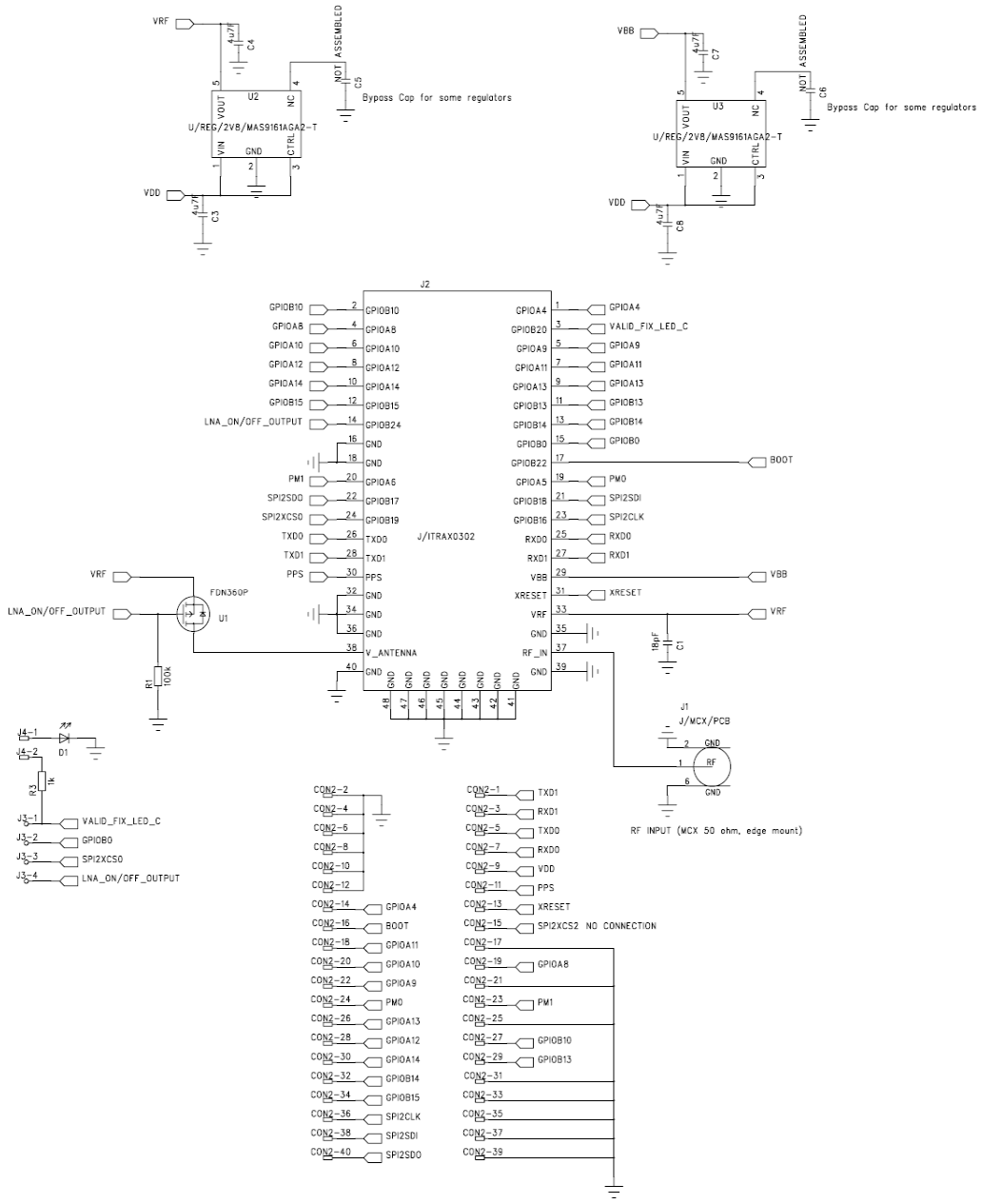


Figure 8 IT03-02 Application Board, Block Diagram.

8.3 I/O Card Terminal connector

The following signals are available at the I/O Card Terminal connector CON2.

Table 9 Card Terminal Connections

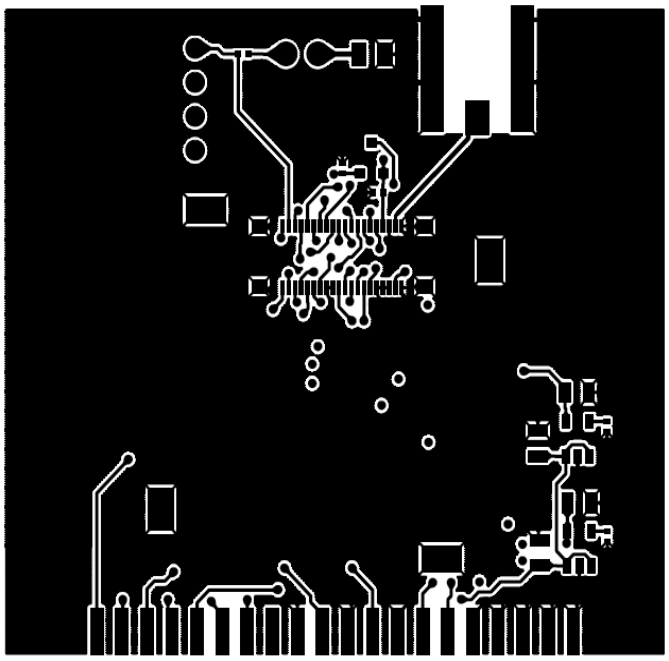
Pin	Signal name	I/O	Alternative GPIO	Signal description
1	TXD1	O	GPIOA3	UART 1 async. output
2	GND	-	-	Ground
3	RXD1	I	GPIOA2	UART 1 async. input
4	GND	-	-	Ground
5	TXD0	O	GPIOA1	UART 0 async. output
6	GND	-	-	Ground
7	RXD0	I	GPIOA0	UART 0 async. input
8	GND	-	-	Ground
9	VCC	-	-	Power input
10	GND	-	-	Ground
11	PPS	O	GPIOA7	1PPS signal output
12	GND	-	-	Ground
13	XRESET	I	-	Active low async. system reset
14	FCLK	O	GPIOA4	Pre-divided clock output of UART 1
15	SPI2XCS2	O	GPIOB21	SPI2 chip select2, (2nd boot select)
16	SPI2XCS3	I/O	GPIOB22	SPI2 chip select3, Boot Select
17	GND	-	-	Ground
18	TCAP1	I	GPIOA11	Timer TMG1 capture input
19	TIN0	I	GPIOA8	Timer TMG0 external clock input
20	TIN1	I	GPIOA10	Timer TMG1 external clock input
21	GND	-	-	Ground
22	TCAP0	I	GPIOA9	Timer TMG0 capture input
23	PM1	I	GPIOA6	Pulse measurement input 1
24	PM0	I	GPIOA5	Pulse measurement input 0
25	GND	-	-	Ground
26	MMCCMD	I/O	GPIOA13	MMC command bus, UI indicator B
27	SPI1XCS0	O	GPIOB10	SPI1 chip select 0, *GPIO reserved for future use. Do not*

28	MMCCLK	O	GPIOA12	MMC clock output
29	SPI1CLK	O	GPIOB13	SPI1 clock
30	MMCDAT	I/O	GPIOA14	MMC data bus, UI indicator A
31	GND	-	-	Ground
32	SPI1SDO	O	GPIOB14	SPI1 data output
33	GND	-	-	Ground
34	SPI1SDI	I	GPIOB15	SPI1 data input, Wake-up input
35	GND	-	-	Ground
36	SPI2CLK	I/O	GPIOB16	SPI2 clock, output in master mode
37	GND	-	-	Ground
38	SPI2SDI	I	GPIOB18	SPI2 data input, On/Off control inp
39	GND	-	-	Ground
40	SPI2SDO	O	GPIOB17	SPI2 data output, UI indicator C
Pin	Signal name	I/O	Alternative GPIO	Signal description

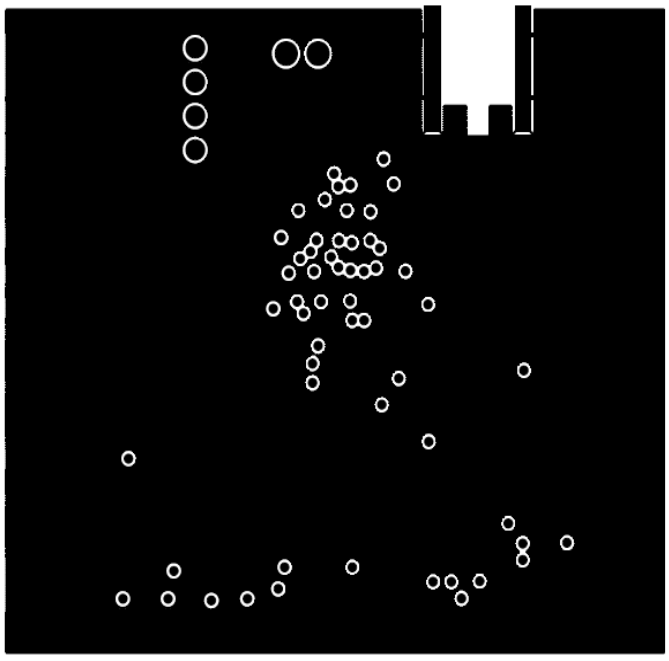
8.4 Bill of Materials

Reference	Value	Qty	Manufacturer	Mfg code	Package	Part type	Description
C2	10n	1			0402	Capacitor	X7R 10%
C5-6	N/A	2			0402	Capacitor	X7R 10%
C1	18p	1			0402	Capacitor	NPO 10%
C3-4 C7-8	4u7	4	MURATA	GRM40-034X5R475K6.3	0805	CAPACITOR	X5R 6.3V
CON2		1	Samtec	EMT-120-01-S-D	SMD	Connector	SOCKET STRIP 40 PINS
J1		1	Huber Suhner	82 MCX-S50-0-22/111NE	Edge mount	Connector	MCX SMD female
U1		1	Fastrax	IT03	SMD module	Module	GPS Receiver
R1	220R	1			0402	Resistor	Resistor, 5%
R2	4k7	1			0402	Resistor	Resistor, 5%
U2-3		2	MAS	MAS9161AGA2-T	TSOT 5	Regulator	LDO
REN1-6	220R	6	Philips	ARV241	0603*4	Resistor	Resistor Array

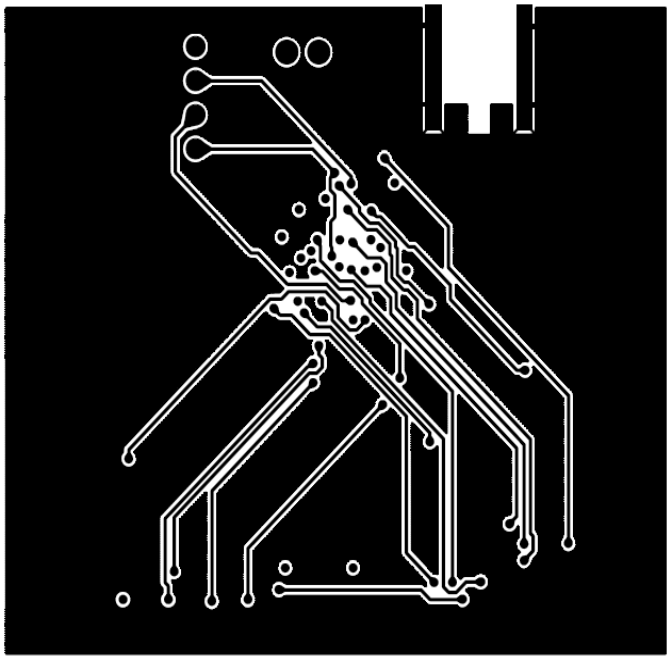
8.5 Application Board, PCB layer 1, Top side



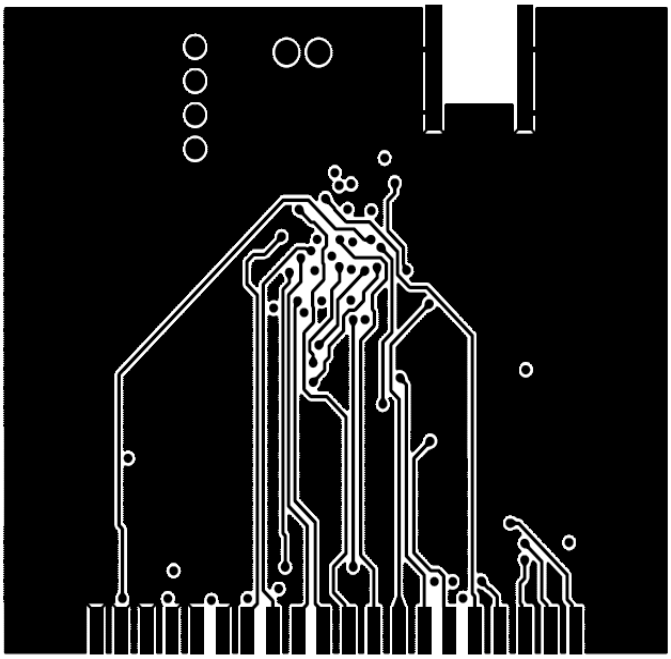
8.6 Application Board, PCB layer 2



8.7 Application Board, PCB layer 3



8.8 Application Board, PCB layer 4, Bottom side



Contact Information

Fastrax Ltd.

Street Address: Valimotie 7, 01510 Vantaa, FINLAND

Tel: +358 (0)424 733 1

Fax: +358 (0)9 8240 9691

http://www.fastraxgps.com

E-mail:

Sales: sales@fastraxgps.com

Support: support@fastraxgps.com