REV 1.6

Technical Description

IT300 GPS Receiver

This document describes the electrical connectivity and main functionality of the IT300 module.

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Fastrax Ltd.

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CHANGE LOG

Rev.	Notes	Date
0.1	Preliminary documentation	2006-01-16
0.2	Updated module height, antenna bias supply voltage, reflow soldering profile	2006-03-09
1.0	Corrected block diagram and operating temperature range, Port A protocol to NMEA, removed SW-boot mode, updated Application Board documentation	2006-04-26
1.1	Added suggestion to use external LNA with passive antennas. Added note on the operation temperature range.	2006-05-18
1.2	Added note on switching between NMEA and SiRF protocols. Updated Minimum Application and IT300 Application Board circuit diagrams (removed *WAKEUP* signal J8 control to VDD regulator)	2006-10-05
1.3	Updated specifications due to transition to SiRF GSC3e/LP chip. Updated block diagram. Corrected table 7. Corrected dimension tolerance and added keep out area. Added tape & reel specification and default firmware configuration, chapter 3.2.1	2006-12-18
1.4	HW revision E: Updated specifications due to transition to SiRF GSC3e/LPx chip, 75mW power. Removed suggestion for external LNA usage with passive antenna. Module name changed to IT300. Updated block diagram. I/O level change to 2.8V CMOS, inputs are 3.3V tolerable. XRESET & ON_OFF inputs are 1.2V CMOS compatible and 3.3V tolerable. Clarifications in low power operation modes.	2009-01-08
1.5	Added chapter 3.3 (Back up state). Corrected chapter 3.4 heading (Power management modes). Added a note on regulator compatibility requirement with low ESR capacitor load. Updated supply voltage range.	2009-01-19
1.6	Corrected default firmware configuration to ***CAR*** variant with single protocol Port A 9600 baud NMEA.	2010-10-01

CONTENTS

COMPLEMENTARY READING

The following reference documents are complementary reading for this document:

Ref. #	File name	Document name
1	Fastrax IT MP Application Note	Fastrax Multiplatform concept

The following SiRF reference documents are also complementary reading for this document.

Ref. #	File name	Document name
I	GSC3LPxProductInsert.pdf	GSC3e(f)/LPx Product Insert
II	NMEA Reference Manual.pdf	NMEA Reference Manual
III	SiRF Binary Protocol Reference Manual.pdf	SiRF Binary Protocol Reference Manual
IV	APNT3008.pdf	SiRF Application Note Power Management Considerations of SiRFstarIII

1 GENERAL DESCRIPTION

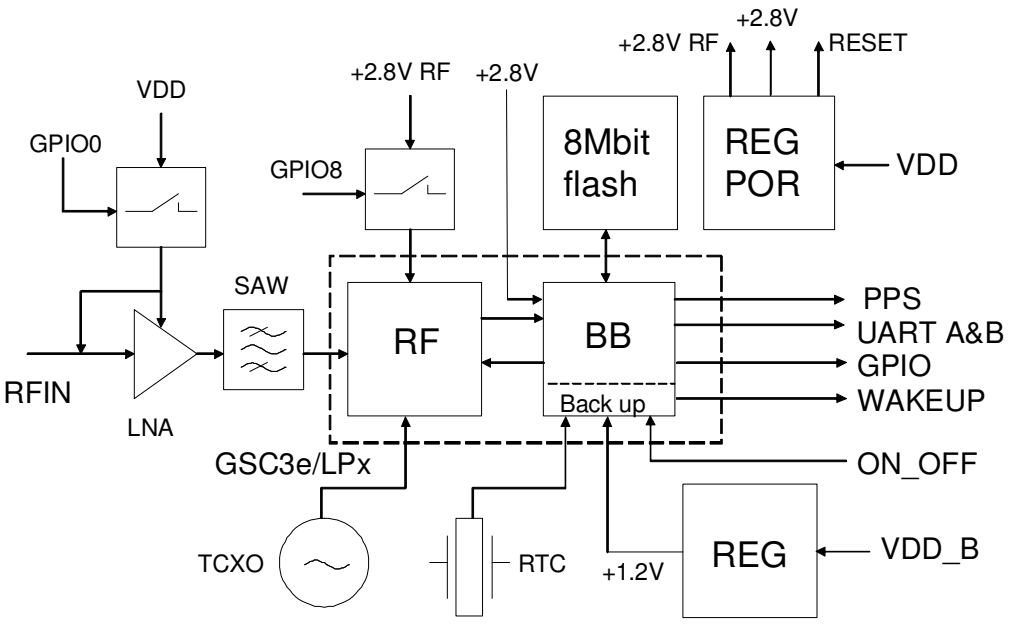
The Fastrax IT300 is an OEM GPS receiver module, which provides the SiRFstarIII receiver (ref I) functionality using the low power SiRF GSC3e/LPx chip together with 8Mbit Flash memory. The module has tiny form factor 16.2x18.8mm, height is 2.3mm nominal (2.5mm max). The IT300 receiver provides low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations. The receiver complies to the Fastrax MP (Multiplatform) connectivity and size, i.e. it is pin compatible to e.g. IT03-S. The module is available with SiRF GSW3 firmware.

The module provides complete signal processing from antenna to serial data output in either NMEA messages (ref II) or in SiRF binary protocol (ref III). A second serial port is also available for differential corrections or for custom purposes. The module requires a power supply VDD, a back up supply voltage VDD_B for non-volatile RTC & RAM blocks and GPS antenna input signal. The IT300 module interfaces to the customer's application via two serial ports, two control signals, PPS timing signal and programmable GPIO signals. Serial data and all I/O signal levels are CMOS compatible.

The antenna input supports passive and active antennas and provides also an internally generated antenna bias supply.

This document describes the electrical connectivity and main functionality of the IT300 module.

1.1 Block diagram



1.2 Frequency Plan

Clock frequencies generated internally at the IT300 receiver:

- 32768 Hz real time clock (RTC)
- 16.369 MHz master clock (TCXO)
- 1571.424 MHz local oscillator of the RF down-converter

2 SPECIFICATIONS

2.1 General

Table 1 General specifications

Receiver	GPS L1 C/A-code, SPS
Channels	20 (12 in tracking, firmware limited)
Update rate	1 Hz default (fix rate configurable with SiRF TricklePower)
Supply voltage, VDD	+3.0V…+3.6 V
Back up supply voltage, VDD_B	+1.5V…+3.6 V (preferably active all the time)
Power consumption, VDD	75 mW typical @ 3.0V (without Antenna bias)
Power consumption, VDD_B	18 uW typical @ 3.0V (during Back up state)
Antenna net gain range	0…+35dB (+10… +35dB suggested for optimum performance)
Antenna bias voltage	Same as VDD
Antenna bias current	150 mA max (must be externally limited at VDD)
Storage temperature	-40ºC…+85ºC
Operating temperature (*note 1*)	-30ºC…+85ºC
Serial port configuration (default)	Port A: NMEA; Port B: SiRF binary
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	NMEA: 9600 baud (SiRF binary 57600 baud)
I/O signal levels	GPIO, UART: 2.8V CMOS compatible: low state 0…0.8V; high state 2.0…2.8V. Inputs are 3.3V tolerable. XRESET, ON_OFF: 1.2V CMOS compatible: low state 0…0.3V; high state 0.9… 1.2V. Inputs are 3.3V tolerable.
I/O sink/source capability	+/- 2 mA max.
PPS output	+/-1us accuracy

Note 1: Usage in the temperature range –40°C… –30°C is accepted but Time-to-First-Fix may be increased.

2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	500	mW
Supply voltage, VDD	-0.3	+5.0	V
Supply voltage, VDD_B	-0.3	+5.5	V
Current output on antenna input	0	+150	mA
Input voltage on any input connection	-0.3	+3.6V	V
RF input level	-	+15	dBm

3 OPERATION

3.1 Operating modes

After power up IT300 boots from the internal flash memory for normal operation. Modes of operation:

- Navigating mode
    - Back up state
    - Power management system modes (TricklePower, Push-to-Fix)
- Programming mode

3.2 Normal mode

The IT300 receiver enters navigating mode after power up. It will start navigation automatically after power up/reset using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM). The power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as Full-power state.

Navigation is available as long as the VDD and VVD_B power supplies are active. Navigation can be stopped by switching VDD off by the host while keeping VDD_B active, which is called also as *Back up* state.

Any configuration settings are valid as long as the back up supply VDD_B is active. When the VDD_B is powered off, the configuration is reset to factory configuration on next power up.

3.2.1 Firmware configuration

Fastrax default SiRF GSW3 firmware configuration *(ref III)*, firmware variant ***CAR***:

1. Port A: NMEA 9600 baud (switchable to binary)
2. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
3. Port B: no protocol
4. Track smoothing: disabled
5. Static navigation: enabled
6. DGPS/SBAS: disabled
7. Datum: WGS84

3.3 Back up state

Back up mode means a low quiescent power state where only the internal non-volatile RTC and RAM block is powered on via VDD_RTC supply. The main supply input VCC is powered off and navigation is halted.

When the main supply VCC is powered on again, the receiver will start navigation automatically with fastest possible TTFF using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM).

3.4 Power management modes

The receiver supports also SiRF operating modes for reduced average power consumption (*ref IV*) like Adaptive TricklePower™ and Push-to-Fix™ modes:

1. *Adaptive TricklePower:* In this mode the receiver stays at Full Power for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in a low power Stand-by state to reduce power drain. TricklePower mode is configurable with SiRF binary protocol message ID151 (*ref III*). The receiver stays once in while in Full Power automatically to collect new ephemeris and almanac data from rising satellites.

2. *Push-to-Fix*: In this mode the receiver is configured to wake up periodically, typically every 1800 sec, to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in a low power CPU only state. The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >62us) after which the receiver performs Hot start and a valid fix is available within few seconds. This mode is configurable with SiRF binary protocol message ID151 (*ref III*).

Note that position accuracy is somewhat degraded in power management modes when compared to full power operation.

3.5 Programming mode

Re-programming via HW-booting mode is utilized by keeping the BOOT control input at low state during power up or at system reset. Now the GPS module boots from the serial data Port A and waits for the boot loader commands from the host (an application running on the host, SIRFFlash). It is suggested that all applications should support the HW-booting by access to serial Port A (TX & RX), BOOT and XRESET signals.

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to the host without any transferring utilities that may cause a failure during speed change.

4 CONNECTIVITY

4.1 Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard in application. All the unconnected I/O should be left open (floating) unless instructed to use pull external up or pull down.

Table 3 Connections

Contact	Signal name	I/O	Alternative signal name	Signal description
1	ON_OFF	I	-	Control input for wakeup from Hibernate/Stand-by states: low-to-high toggle >62us. Can be used only in Hibernate/Stand-by states (Push-to-Fix). Pull low externally with e.g. 10k resistor if not used. (4)
2	BOOT	I	-	Boot control input: 0=UART, 1=Internal flash memory. Pull high externally with 4k7-100k resistor. (3)
3	GPIO14	I/O	-	(1) (3)
4	GPIO2	I/O	-	(2) (3)
5	GND	I/O	-	Ground
6	GPIO15	I/O	-	(1) (3)
7	GPIO4	I/O	-	(3)
8	WAKEUP	Od	-	Open drain output for VDD control, use pull up resistor, max pull up voltage +3.6V. Can be left unconnected if not used. Reserved for future usage.
9	XRESET	I	-	Asynchronous system reset, active when low 0... 0.3V. Pulled high to VDD with internal 100kohm resistor. Can be left unconnected if not used. (4)
10	n.c.	-	-	Not connected
11	GND	-	-	Ground
12	GPIO13	I/O	-	(3)
13	GPIO1	I/O	-	(2) (3)
14	VDD_B	I	-	Power supply for battery back up
15	GND	-	-	Ground

16	TXDB	O	-	UART B async. output (3)
17	TXDA	O	-	UART A async. output (3)
18	RXDA	I	-	UART A async. input (1) (3)
19	RXDB	I	-	UART B async. input (1) (3)
20	GND	-	-	Ground
21	n.c.	-	-	Not connected
22	GND	-	-	Ground
23	GND	-	-	Ground
24	RFIN	I/O	-	Antenna signal input, Antenna bias voltage output
25	GND	-	-	Ground
26	GND	-	-	Ground
27	GPIO10	I	EIT[0]	User defined external interrupt, pull high externally with e.g. 10kohm resistor (3)
28	VDD	I	-	Power supply
29	GPIO8	O	RFPWRUP	Dedicated internally for RF power control (3)
30	PPS	O	GPIO9 (2)	1PPS signal output (3)
Contact	Signal name	I/O	Alternative GPIO name	Signal description

Notes:

(1) Has internal 100kohm pull up resistor to +2.8V

(2) Has internal 100kohm pull down resistor to GND

(3) +2.8V CMOS compatible signal levels. Input is +3.3V tolerable.

(4) +1.2V CMOS compatible signal levels. Input is +3.3V tolerable.

4.2 Power supply

The IT300 module requires two separate power supplies: VDD_B for non-volatile back up block (RTC/RAM) and the VDD for digital parts and I/O. RF and digital sections have internally regulated +2.8V supplies. VDD can be switched off when navigation is not needed but if possible keep the back up supply VDD_B active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Back up supply VDD_B draws typically 6uA current in back up state. During navigation VDD_B current may peak up to 70uA typ.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typical VDD peak current is 32mA during acquisition after power up.

Both power inputs have internal ceramic, low ESR capacitors. Use a power supply or regulator that is compatible with low ESR (~ 0.01 ohm) ceramic output load capacitors.

NOTE

Use a power supply or regulator that is compatible with low ESR (~ 0.01 ohm) ceramic output load capacitors.

4.3 Reset

The reset input XRESET is an active low asynchronous reset. The processor boots after the low-to-high transition depending on the state of the BOOT signal. The XRESET input contains an internal voltage detector to force reset during power up or power down transitions.

The input has internal 100k pull up resistor to VDD. For normal operation the XRESET input can be left unconnected.

NOTE

XRESET input is CMOS 1.2V compatible. For proper reset pull input below 0.3V. The input is 3.3V tolerable and is pulled high with internal 100kohm resistor to VDD.

4.4 Boot Select

The boot source is defined in the internal boot ROM sector by using the BOOT control input. After power up or after system reset the value is read and the boot is processed according the following table.

Table 4 Boot select

BOOT	I/O	Boot source
high	I	Boot for internal flash memory (Normal operation)
low	I	External boot UART Port A for re-programming

Boot select should be kept valid after power up for at least 500 ms to allow the internal power-on-reset delay to settle.

In Navigating mode the Boot Select should be kept valid for at least 10us after XRESET low-to-high transition.

NOTE

To ensure normal operation during system reset and power on, the BOOT input requires an external pull-up resistor connected to VDD, e.g. 4.7kohm-100kohm.

4.5 ON_OFF control input

The ON_OFF control input can be used to wake up from Stand-by or Hibernate states during Push-to-Fix operation. The wake up interrupt is generated by a low-high-low pulse, which should be longer than 62us. The input is 1.2V CMOS compatible and also 3.3V tolerable.

NOTE

If not used, pull ON_OFF signal to low state.

4.6 WAKEUP control output

Normally the VDD supply is active during the Push-to-Fix operation. The WAKEUP control output is reserved for future usage in Push-to-Fix operation mode to enable a low quiescent *Hibernate* state, which is in practice the same as *Back up* state but from which the module is able to wake up autonomously after elapsed time or via ON_OFF interrupt. In this Push-to-Fix operation with Hibernate state, the WAKEUP control output is used externally to switch on/off the VDD power supply. The Hibernate state is reserved for future usage.

The output is open drain and if used, it should be pulled up with a suitable resistor. The polarity is active low, i.e. the VDD should be active when WAKEUP signal is low.

NOTE

If used, a suitable pull up resistor should be used around 100kohm; check with the used VDD regulator. Max pull up voltage is +3.6V

4.7 Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides also a bias supply (the same as VDD). When the navigation is stopped, the antenna bias is switched off internally.

The maximum tolerated antenna bias current is 150mA, which shall be current limited by the external regulator supplying VDD.

NOTE

Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

4.7.1 Active GPS antenna

The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range from +10 dB to +35 dB.

NOTE

Antenna bias current from VDD supply should be limited externally to 150 mA max.

4.8 UART

The device supports UART communication via Port A and Port B. With the standard firmware variant ***CAR*** the Port A is configured by default to NMEA protocol with 9600 baud and Port B has no protocol; this allows Port A switching to SiRF binary (e.g. at 57600 baud) by a NMEA command (*ref II*). The Port A is used also when the device is booting from the serial port for re-programming.

The default configuration for Ports and respective protocols can be changed by commands via NMEA or SiRF binary protocols *(ref II & III)*. Any custom configuration settings stay active as long as the back up supply VDD_B is active.

I/O levels form the serial ports are 2.8V CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed. Inputs are 3.3V tolerable.

4.9 Dedicated GPIO

Some of the GPIOs have a shared or dedicated functionality. Each signal is named according to the main functionality but also the secondary functionality is listed as the Alternative signal name.

All GPIO's are configured to inputs by default after system reset, except GPIO8 RFPWRUP, which is configured to output. I/O levels from GPIO are 2.8V CMOS compatible and inputs are 3.3V tolerable.

4.9.1 GPIO0

GPIO0 is reserved internally for power control of the low noise amplifier (LNA) and antenna bias supply. The signal is not available at the external I/O connections.

4.9.2 PPS/GPIO9

The pulse-per-second (PPS) output provides an output for timing purposes. It shares the PPS functionality with GPIO9 for custom purposes.

4.9.3 GPIO8/RFPWRUP

The GPIO8 is dedicated internally for controlling the supply voltage for the RF block and for TCXO master clock. The output can be used for monitoring purposes of the state of the baseband block.

4.9.4 GPIO10/EIT[0]

The GPIO10/EIT[0] is the only user definable interrupt capable input, which is available only in Full-power or CPU-only states. If not used, it should be pulled high.

NOTE

If not used, pull GPIO10/EIT[0] signal to high state.

4.10 Mechanical dimensions and contact numbering

Module size is 16.2mm (width) x 18.8mm (length) x 2.3mm (height 2.5mm max). General tolerance is ±0.2mm.

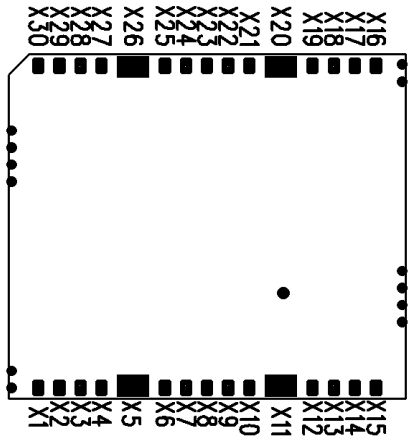


Figure 1 Contact numbering, top view.

4.11 Suggested pad layout

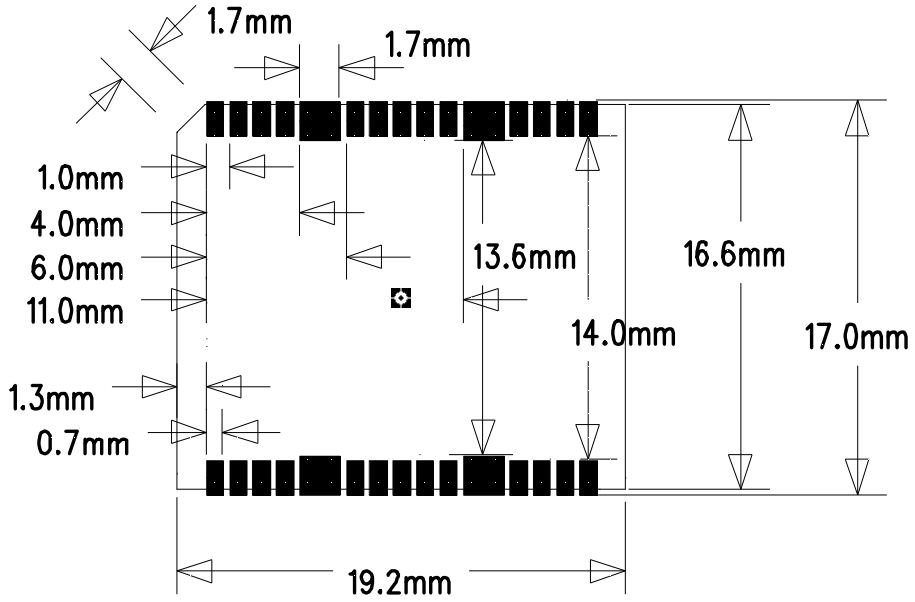


Figure 2 Suggested pad layout and occupied area, top view.

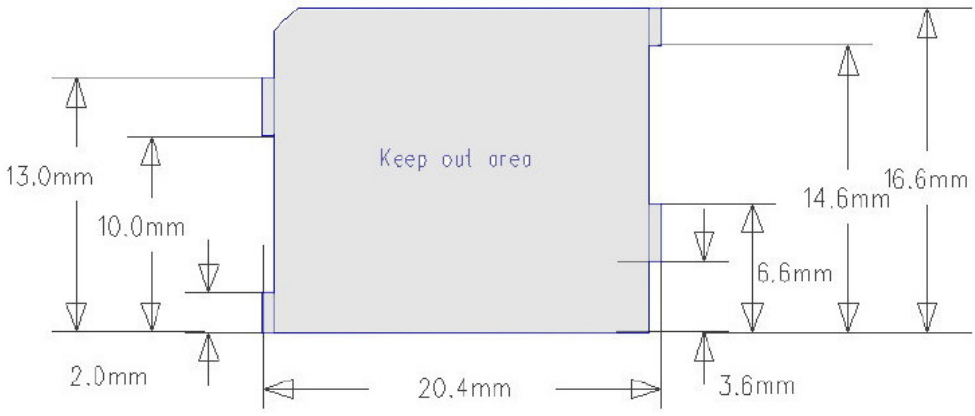


Figure 3 Suggested component keep out area, top view.

5 MANUFACTURING

5.1 Assembly

The IT300 module supports only assembly and soldering in a reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume.

5.2 Suggested Reflow soldering profile

Suggested reflow peak temperature is 235… 245ºC for 5 seconds (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC.

5.3 Moisture sensitivity

Note that the IT300 is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

5.4 Tape and reel

One reel contains 500 modules.

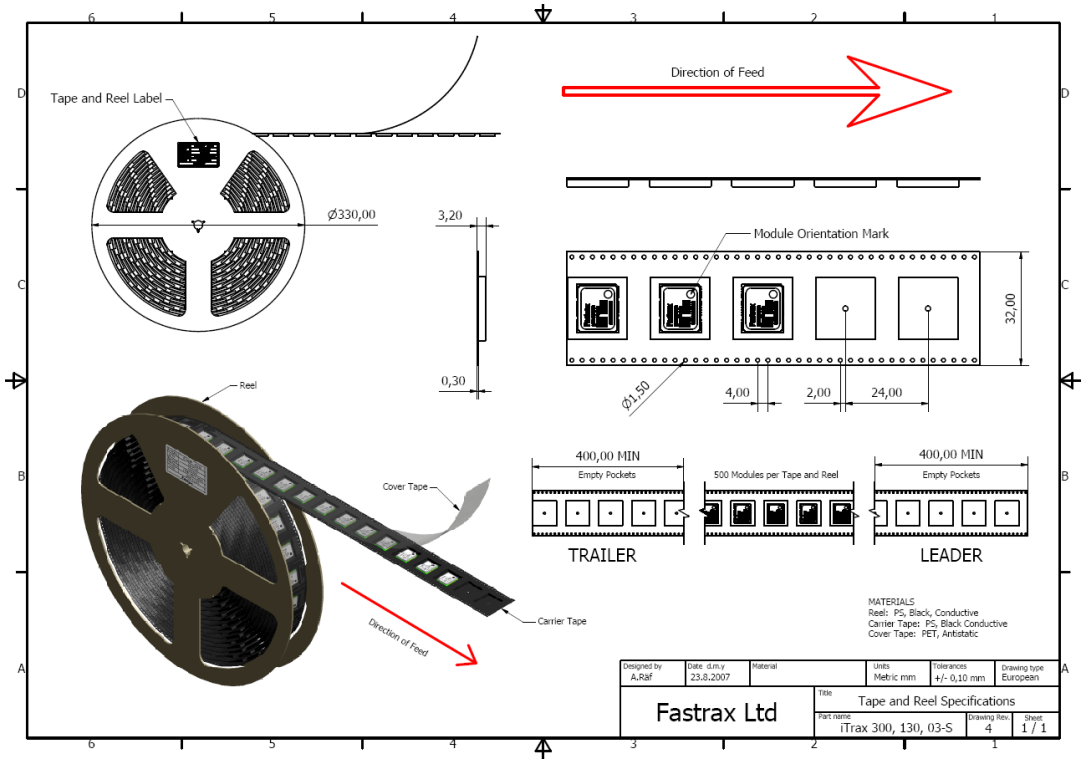


Figure 4 Tape and reel specification

6 REFERENCE DESIGN

The idea of the reference design is to give a guideline for the applications using the IT300 GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing an IT300 in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

6.1 Minimum Application Circuit Diagram

The Minimum Application supports communication through the UART Port A (NMEA protocol).

NOTE

With default firmware configuration (**STD** variant) the Port A supports only NMEA protocol and it is not possible to switch Port A to SiRF binary protocol since it is already present at Port B. If customer wants to use only UART Port A for switching between NMEA and SiRF binary protocols, request the module with a different firmware variant (e.g. **CAR**) with single NMEA protocol at Port A.

Other required signals are the antenna input, supply voltage for VDD and VDD_B, GND, a pull-up resistor for the BOOT control signal and pull down resistor for ON_OFF control signal. Also the GPIO10/EIT[0] is pulled high.

The low drop-out linear regulator (LDO) U3 supplies +3.0 V voltage to VDD. The C6 provides back up supply to VDD_B. The back up supply can be provided also from a suitable coin cell battery or from any available back up supply with suitable voltage range.

All the digital signals are routed away from the module through series resistors (R1, R2, R3). In this way the local oscillator (LO) signal leakage that is present in the I/O contacts of the GPS module is suppressed. Although the LO leakage is very small at the IO contacts of the module, it may still interfere the GPS reception, especially when the antenna is located very near to these signal routes. Place these series resistors and also pull up resistors R14, R15 and R16 with short traces close to the module.

For the same reason capacitors C1 and C2 should be connected very close to the module with short traces to I/O contacts and to ground plane.

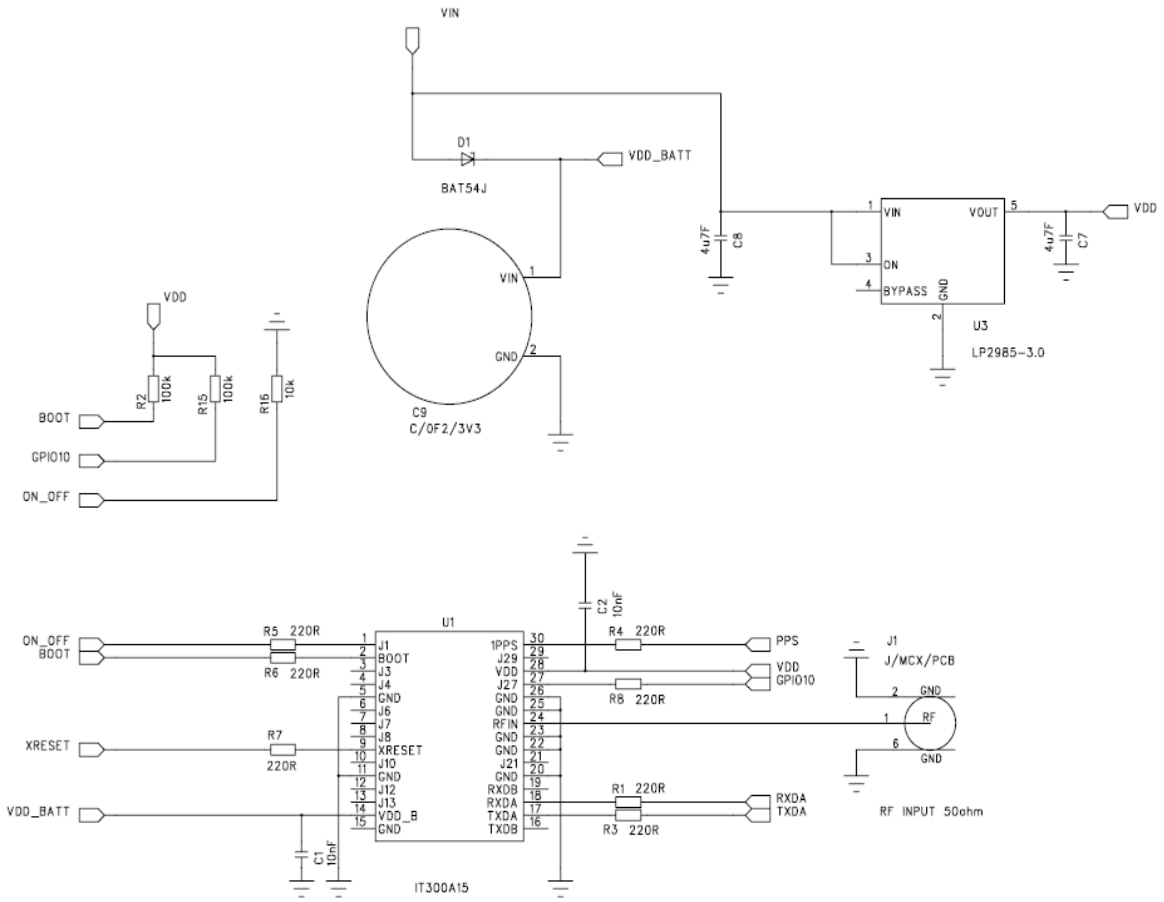


Figure 5 Minimum Application Circuit Diagram.

Note that there is a DC bias voltage present at the RF input, when the module is operating in Navigating mode. If a passive antenna with a short-circuit to the GND is used, an external series DC block capacitor (18pF…1nF) must be used for the RFIN signal line.

6.2 PCB layout issues

The suggested 4-layer PCB build up is presented in the following table.

Table 5 Suggested PCB build up

Layer	Description
1	Signal + Ground with copper keep-out below IT300
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT300 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed very near to the IT300 module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C1 and C2 should be connected very close to the module's with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT300 to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes per GND pad.

The RF input should be routed clearly away form other signals, this minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

7 IT300 APPLICATION BOARD

The IT300 Application Board provides the IT300 connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the IT300 module, one regulator for VDD supply, a 0.2F capacitor for VDD_B back up supply, an MCX antenna connector and a 2x20 pin Card Terminal connector.

7.1 Card Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. Note that serial Port A and B maps to Port 0 and 1 at the Evaluation Kit, respectively.

Table 6 IT300 Application Board connectivity

Pin	Signal name	I/O	Alternative GPIO	Interface to Fastrax Evaluation Kit
1	TXDB	O	-	UART 1 async. output
2	GND	-	-	Ground
3	RXDB	I	-	UART 1 async. input
4	GND	-	-	Ground
5	TXDA	O	-	UART 0 async. output
6	GND	-	-	Ground
7	RXDA	I	-	UART 0 async. input
8	GND	-	-	Ground
9	VDD	I	-	Power input +3.3V
10	GND	-	-	Ground
11	PPS	O	GPIO9	1PPS signal output
12	GND	-	-	Ground
13	XRESET	I	-	Active low async. system reset
14	-	-	-	Not connected
15	-	-	-	Not connected
16	BOOT	I	-	Boot Select
17	GND	-	-	Ground
18	GPIO2	I/O	-	Led Indicator D7
19	GPIO4	I/O	-	Led Indicator D4

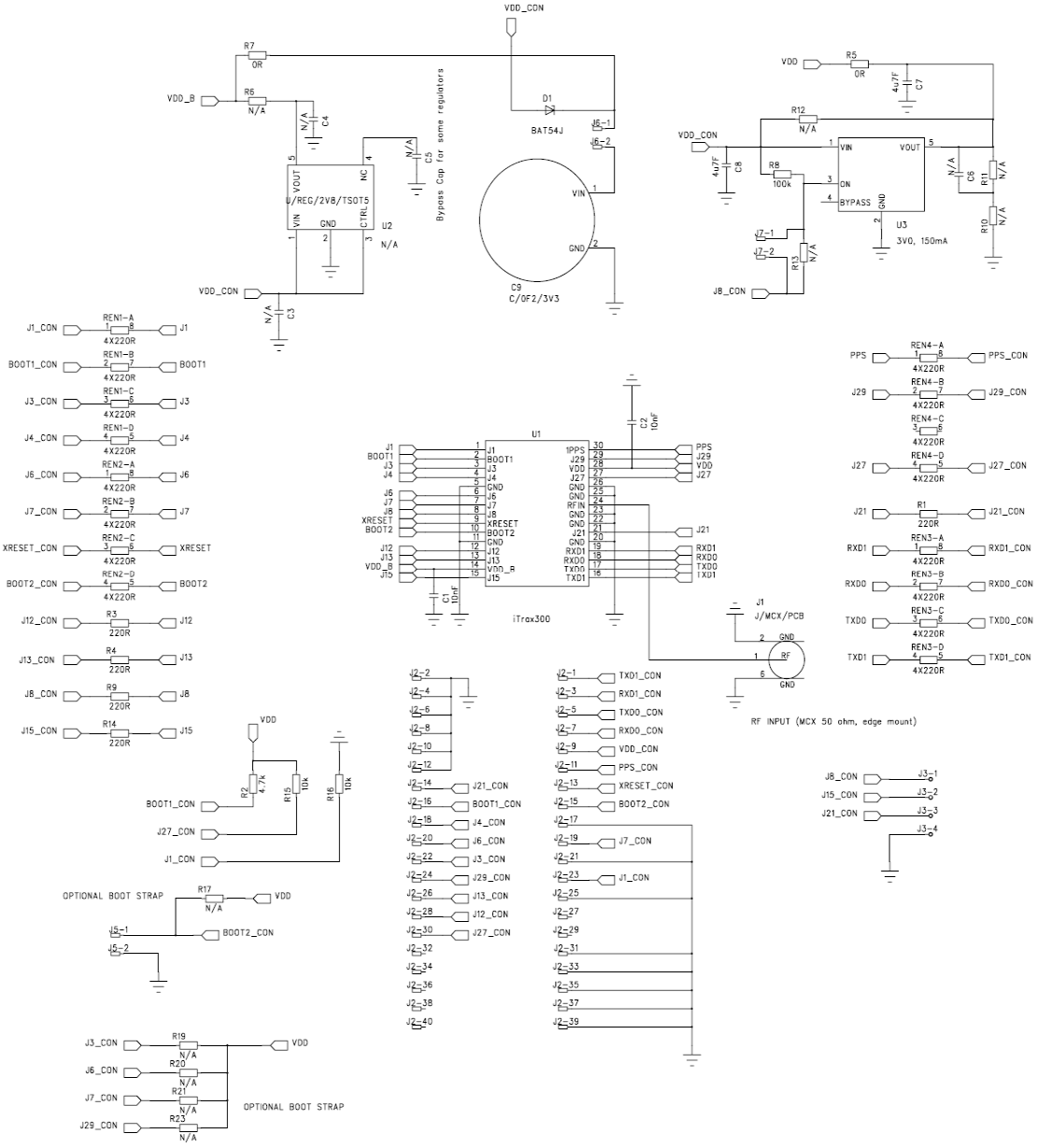
20	GPIO15	I/O	-	Led Indicator D6
21	GND	-	-	Ground
22	GPIO14	I/O	-	Led Indicator D5
23	ON_OFF	I	-	Led Indicator D3
24	RFPWRUP	O	GPIO8	Led Indicator D2
25	GND	-	-	Ground
26	GPIO1	I/O	-	User Interface Indicator UI_ B
27	-	-	-	Not connected
28	GPIO13	I/O	-	Led Indicator D8
29	-	-		Not connected
30	EIT[0]	I	GPIO10	User Interface Indicator UI_A
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	-	-	Not connected
35	GND	-	-	Ground
36	-	-	-	Not connected
37	GND	-	-	Ground
38	-	-	-	Not connected
39	GND	-	-	Ground
40	-	-	-	Not connected
Pin	Signal name	I/O	Alternative GPIO	Interface to Fastrax Evaluation Kit

7.2 Bill of materials

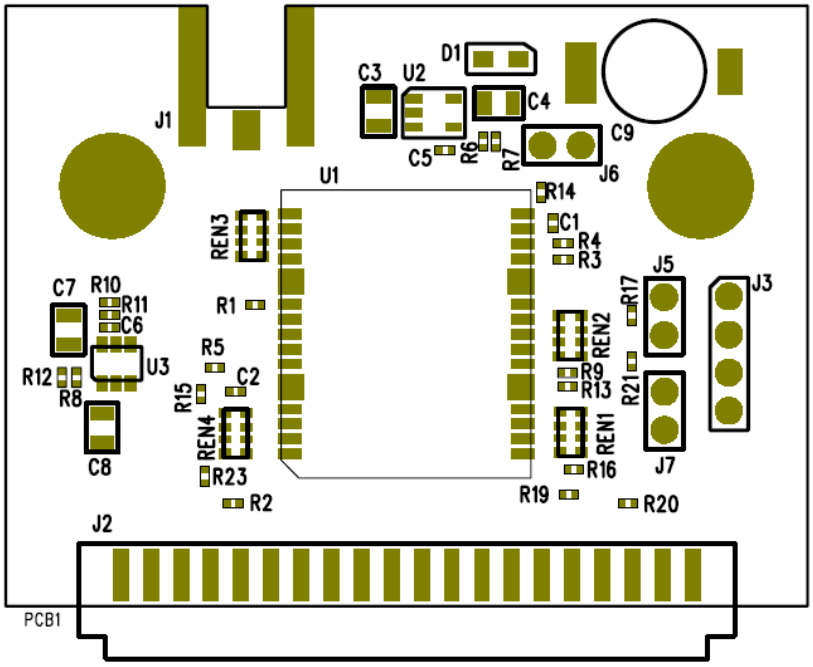
Table 7 Bill of materials

Qty	Reference	Part Name	Description
1	C6	CAPACITOR CHIP	N/A
1	C1	CAPACITOR CHIP	10nF 16V 10% X7R 0402
1	C2	CAPACITOR CHIP	10nF 50V 10% X7R 0402
1	C5	CAPACITOR CHIP	10nF 50V 10% X7R 0402
2	C7-8	CAPACITOR CHIP	4,7uF 6,3V X5R 0805 +-20%
2	C3-4	CAPACITOR CHIP	4,7uF 6,3V X5Y 0805
1	C9	CAPACITOR	CAP BACKUP 0.2F 3V3
1	D1	DIODE	Diode 75V 225mA, BAT54J
2	H3-4	PCB ACCESSORIES	FIDUCIAL, Circle, rectangle, triangle
2	H1-2		
1	U1	HIERACHY	iTrax300 module
1	J6	CONNECTOR	1x2 pin-header, straight, 2,54mm
2	J5 J7	CONNECTOR	1x2 pin-header, straight, 2,54mm
1	J3	CONNECTOR	1x4 pin-header, straight, 2,54mm
1	J2	CONNECTOR	EDGE MOUNT SOCKET STRIP 40 PINS
1	J1	Connector	50 Ohm male MCX connector PCB
1	PCB1	PCB	Application board for iTrax MP, Rev. A00
2	R5 R7	RESISTOR CHIP	0R 0402
1	R6	RESISTOR CHIP	0R 0402
1	R13	RESISTOR CHIP	N/A
1	R12	RESISTOR CHIP	0R 0402
1	R8	RESISTOR CHIP	100k 5% 0402 63mW
2	R15-16	RESISTOR CHIP	10k 5% 0402 63mW
5	R17 R19-21 R23	RESISTOR CHIP	10k 5% 0402 63mW
5	R1 R3-4 R9 R14	RESISTOR CHIP	220R 5% 0402 63mW
1	R10	RESISTOR CHIP	N/A
1	R11	RESISTOR CHIP	N/A
1	R2	RESISTOR CHIP	4.7k 5% 0402 63mW
4	REN1-4	RESISTOR CHIP ARRAY	4 x 220R ARV241
1	S1	SWITCH	Jumper, Pitch, 2.54mm, Red colour
1	U2	IC Regulator	N/A
1	U3	IC REGULATOR	TI: LP2985-30DBVR, NSC: LP2985IM5X-3.0

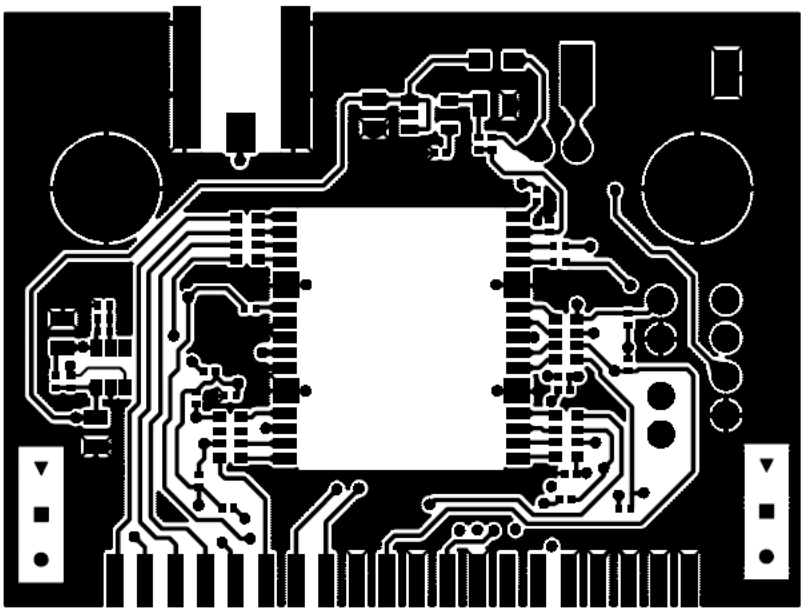
7.3 Circuit drawing



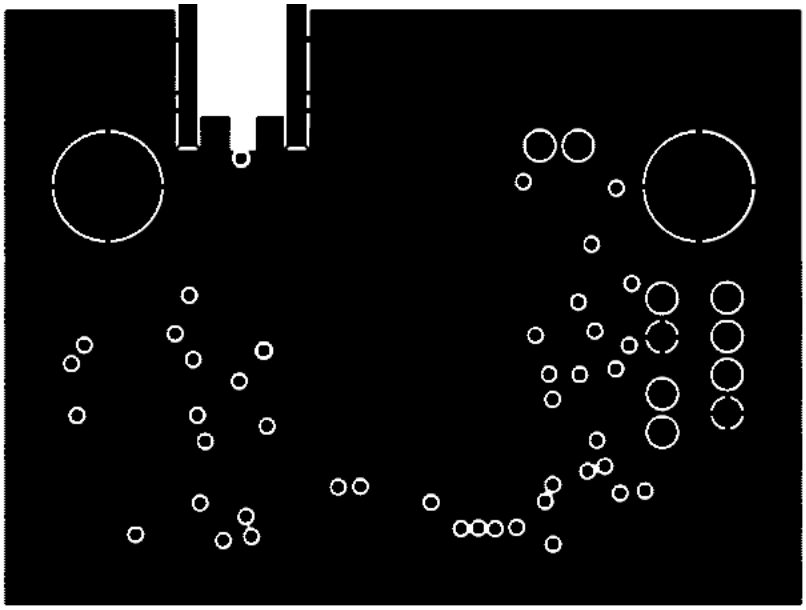
7.4 Assembly drawing, Top side



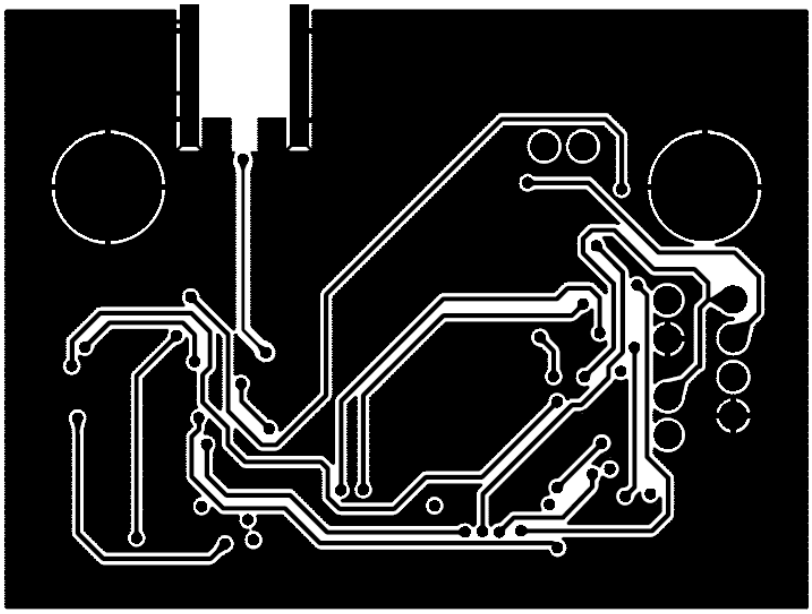
7.5 Artwork, layer 1 (Top)



7.6 Artwork, layer 2



7.7 Artwork, layer 3



7.8 Artwork, layer 4