Rev 1.3

APPLICATION NOTE

IT MP Family

This document describes how to achieve common connectivity and functionality of the IT MP GPS receivers.

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Fastrax Ltd.

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CHANGE LOG

Rev.	Notes	Date
0.1	Initial document	2006-01-19
0.2	Merged new material	2006-02-01
0.3	Corrected general specifications	2006-02-03
0.4	Added pull up R5 to Application Circuit, added Simple Application Circuit	2006-02-17
0.5	Updated module heights, corrected Application Circuit diagrams (J27 pull up resistor R5, R2 pull up value 4.7kohm)	2006-03-09
0.6	Updated performance specifications and regulator suggestions, added notes on Back up state versus I/O	2006-03-10
1.0	Clarified tables and presentation with common module order, corrected iTrax130 pin out. Added suggestion for an external LNA with passive antennas. Updated general specifications.	2006-05-18
1.1	Updated specifications, added suggested component keep out area (Fig 3.)	2007-01-08
1.2	Corrected Sony chip numbering and iTrax130 pin out picture	2007-01-09
1.3	- New module naming: iTrax changed to IT. - IT130 removed (EOL). - IT500 added. - IT300 data and operation updated.	2009-09-11

Contents

COMPLEMENTARY READING

The following reference documents are complementary reading for this document. All operating and firmware related documentation is also available at ***www.fastraxgps.com***

Ref. #	File name	Document name
1	IT300_Tech_doc.pdf	IT300 Technical Description
2	IT500_Tech_doc.pdf	IT500 Technical Description
3	IT03-S_Tech_doc.pdf	IT03-S Technical Description
4	Reflow_soldering_profile.pdf	Module Soldering Profile

1. GENERAL DESCRIPTION

1.1 IT MP concept

The IT MP Family consists of three high performance OEM GPS receiver modules, namely IT03-S, IT300 and IT500, which share the common connectivity and size with a tiny form factor 16.2mm (typ.) x 18.8mm (typ.) x 2.5mm (max).

IT MP allows designers to address several customer and market requirements with a single hardware design thus saving considerable amount of development, testing, documentation and support cost while reducing time to market to an absolute minimum. The market demand for best performance, lowest possible cost and lowest power consumption can now be addressed with a single hardware design. The IT MP concept also reduces single source risks.

All modules provide complete signal processing from antenna to serial data output in either NMEA messages or in proprietary binary protocols. A second serial port is available for custom purposes. All modules require a dual power supply and a GPS antenna input signal. Serial data and all I/O signal levels are CMOS compatible. The pin out of each module is chosen so that common signals like power supplies, antenna input, reset & boot control signals and serial ports have common connectivity.

The IT MP receivers can interface to the customer's application via versatile I/O and supports also several peripherals including a capture timer input, a pulse measurement input, a high speed SPI-bus, a MMC bus and active antenna detector output. The peripherals may have a shared functionality with a General Purpose Input/Output (GPIO). The number of GPIO's and availability of the peripherals depends on the receiver type.

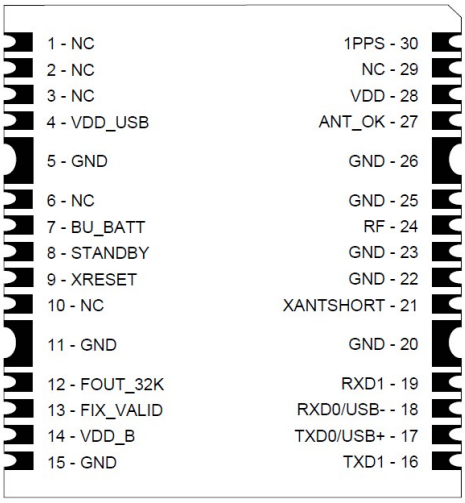
This document describes how to achieve common connectivity and functionality with the IT MP receivers.

1.2 IT MP compatible receivers

- **IT300** is based on SiRF GSC3e/LPx single chip
- **IT500** is based on MediaTek MT3329 single chip
- **IT03-S** is based on Atheros uN8021 RF IC and uN2100 BB LSI

The pin-outs for all modules are shown below. The following pins needs attention when designing a user application using any of the three modules:

- Power supplies (battery backup vs. VDDRF supply)
- Control signals for low power modes (Sleep or Backup state)
- Firmware upgrading using UART Port 0 (Port A), XRESET and BOOT1 signals (BOOT1 not applicable with IT500)



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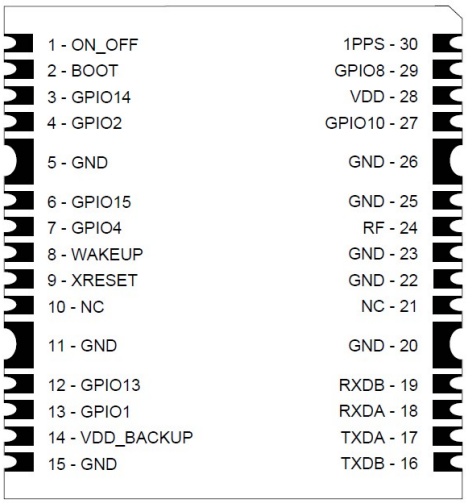
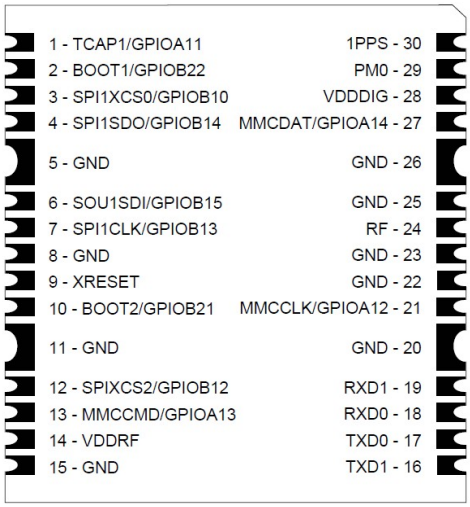


IT300



IT03-S

2. SPECIFICATIONS

2.1 Summary of General Specifications

Table 1 General Specifications

		IT500	IT300	IT03-S
General:	L1, C/A Code, SPS	22 + 66 channels	20 channels	12 channels
Update rate:		1 fix/s (user configurable)	1 fix/s	1 fix/s (user configurable)
Accuracy:	Position:	1.8m (CEP)	1.8m (CEP)	3m (CEP), 8m (2dRMS)
	Velocity:	0.1m/s	0.1 m/s	0.2m/s RMS
	Time:	+/- 50ns RMS	+/-1us	+/-20ns RMS
TTFF:	Cold Start:	34s typ.	32s typ.	35s typ.
	Warm Start	33s typ.	32s typ.	34s typ.
	Hot start:	1s typ.	1s typ.	4s typ.
Sensitivity:	Acqusition (cold):	-148dBm	-146dBm	-142dBm
	Navigation:	-165dBm	-159dBm	-156dBm
	Re-acquisition	-160dBm	-157dBm	-149dBm
Power Drain:	Navigating 1 fix/s:	75mW typ.	75mW typ.	95mW typ.
	Stand-by state:	3mW typ.	3mW typ.	15mW typ.
	Back Up/Sleep state:	15uW typ.	18uW typ.	20uW typ.
Operating voltage:	Main Supply:	+3.0V...4.2V	+3.0V...3.3V	+2.7V..3.3V
	Back up Supply:	+2.0V...4.2V	+1.5V...3.3V	-
	RF Supply:	-	-	+2.7V...3.3V
Other:	Operating temperature:	-40C..+85C	-40C..+85C	-40C..+85C
	Height	2.3mm (2.5mm max)	2.3mm (2.5mm max)	2.3mm (2.5mm max)
	Serial ports:	2	2	2
	GPIO, number of:	5	7 free, 1 dedicated	17 (shared functionality)
	Peripherals:	Antenna detector	-	SPI, MMC, Timer, PM
	SBAS	WAAS/Egnos/MSAS	WAAS/Egnos	WAAS/Egnos
	Chip set	MediaTek MT3329	SiRFstarIII GSC3e/LPx	uNav uN8021+uN2110
	Firmware	AXN 1.3	SiRF GSW3	Fastrax iSuite 3
	Memory	4Mbit Flash	8Mbit flash	8Mbit flash

Sensitivity performance IT03-S is based on the iSuite 3 rev. 3.31 firmware. The IT300 results are based on the SiRF GSW3.5.0. The IT500 performance results are based on MTK AXN1.3 release firmware. Specifications are subject to change without notice.

The main operational differences between the receivers are the power supplies and the controlling of the low power modes.

3. OPERATION

3.1 Operating modes

After power up IT MP receivers boot from the internal flash memory for normal (navigating) operation. Modes of operation:

- Navigating/Idle mode
- Sleep/Backup state
- Programming mode

3.2 Navigating/Idle mode

The IT MP receivers enter navigating mode after power up. They will start navigation automatically after power up/reset using all the available aiding information (GPS time estimate from RTC and Last Known Good position from RAM blocks). The module runs as long as the power supply is available.

Idle & 'CPU only' mode means that the navigation is stopped but the processor remains still active. Navigating mode is also referred as ***Normal*** and ***Full Power*** Mode depending on the receiver.

3.3 Sleep/Backup state

The Sleep/Backup state means a low quiescent operation during which no other activity other that the internal real time clock (RTC + RAM) is present.

With IT300 and IT500 the Backup state is entered when main supply VDD is switched off (controlled by the host). At the same time the backup supply VDD_B is kept active all the time. For details see *ref 1 and 2*.

With IT03-S Sleep state both power supplies are active but the module is configured to low quiescent Sleep state via a command or via a control signal input (On/Off, J4), for details see *ref 3*.

Exit from the Sleep state happens after pre-determined elapsed time or after host wake up interrupt via a control input (J1 or J6). Since the internal RTC keeps the GPS time estimate, the module performs the fastest possible navigation start depending on the availability of valid satellite/position data.

3.4 Programming mode

The module enters programming mode either by an external reset with Boot signals pulled to ground (HW-boot mode), or by a protocol command issued by the flashing utility (Software boot mode), for details see *ref 1, 2 and 3*. HW-boot mode is not available with IT500 and therefore the IT MP BOOT1 connection can be left unconnected with IT500.

The Software boot mode requires only a serial port and the downloading will be started by sending a special command and the utility running on the host will send the new firmware to the processor.

HW-booting is utilized by keeping the BOOT1 control input at low state during power up or system reset. Now the receiver boots from the serial data Port 0 (or A) and waits the for the boot loader commands from the host (a flash utility running on the host). This mode is required when there is no existing firmware stored to the internal Flash memory or when the previous firmware is corrupted.

It is suggested that all applications should support also HW-booting by access to serial Port 0 (A) (both TX & RX signals), BOOT1 and XRESET signals.

NOTE

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to the host without any transferring utilities that may cause a failure during speed change. Use an external MUX for Port 0 (A) to switch between normal serial port usage and reprogramming via a service/production connection.

4. CONNECTIVITY

4.1 Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard of the application. All the unconnected I/O should be left open (floating) unless otherwise stated.

The user is suggested to pay attention especially to the connectivity of the power supplies (back up supply vs. RF supply), to HW-boot mode via serial Port 0 controlled with BOOT1 and XRESET signals and to control signals (J4, J6, J8) for low power operating modes. For suggested connectivity see also the chapter 6, Reference Design.

Table 2 IT MP Connections

	IT MP	**IT500**			**IT300**			**IT03-S**		
Pin	Signal	Signal	Alternate	Note	Signal	Alternate	Note	Signal	Alternate	Note
1	J1	NC			ON_OFF		use 10k pull down	TCAP1	GPIOA11	
2	BOOT1	NC			BOOT		Boot, pull high	BOOT1	GPIOB22	Boot, pull high
3	J3	NC			GPIO14	nRTS		SPI1XCS0	GPIOB10	
4	J4	NC	VDD_USB	With IT500U	GPIO2			SPI1SDO	GPIOB14	On/Off input
5	GND	GND			GND			GND		
6	J6	NC			GPIO15	YCLK		SPI1SDI	GPIOB15	Wake Up input
7	J7	BU_BATT			GPIO4			SPI1CLK	GPIOB13	
8	J8	STANDBY			WAKEUP		output, open drain	GND		
9	XRESET	XRESET			XRESET			XRESET		
10	BOOT2	NC			n.c.		not used	BOOT2	GPIOB21	float or pull low
11	GND	GND			GND			GND		
12	J12	FOUT_32K		1V2 CMOS	GPIO13	nCTS		SPI1XCS2	GPIOB12	UI_C output
13	J13	FIX_VALID			GPIO1	Odometer		MMCCMD	GPIOA13	UI_B output
14	VDD_B	VDD_BACKUP			VDD_BACKUP		Backup supply	VDDRF		RF supply
15	J15	GND			GND			GND		
16	TXD1	TXD1			TXDB			TXD1	GPIOA3	
17	TXD0	TX0/USB+			TXDA			TXD0	GPIOA1	
18	RXD0	RX0/usb-			RXDA			RXD0	GPIOA0	
19	RXD1	RXD1			RXDB			RXD1	GPIOA2	
20	GND	GND			GND			GND		
21	J21	XANTSHORT			n.c.			MMCCLK	GPIOA12	
22	GND	GND			GND			GND		
23	GND	GND			GND			GND		
24	RFIN	RF			RFIN			RFIN		
25	GND	GND			GND			GND		
26	GND	GND			GND			GND		
27	J27	ANT_OK			GPIO10	EIT[0]	pull high	MMCDAT	GPIOA14	UI_A output
28	VDD	VDD			VDD		Digital supply	VDDDIG		Digital supply
29	J29	NC			GPIO8	RFPWRUP	RF PWR control	PM0	GPIOA5	
30	PPS	PPS			1PPS	GPIO9		PPS	GPIOA7	

4.2 I/O naming convention

IT MP receiver signal naming convention in table 2 reflects the compatible signal names for each module. Other signals like GPIO are named according to the contact number (e.g. J1) as each GPIO name may differ for each receiver.

The IT03-S and IT300 uses quite similar control signal names (WAKEUP vs. Wake Up, also ON_OFF vs. On/Off) but the operation of these signal is different. The naming of the IT03-S signals is the original convention. However, the naming of IT300 signals is based on the SiRFstarIII naming convention for clarity with SiRF firmware operation. Be careful when using these control signals to avoid mistakes.

4.3 Power supply

The IT MP modules require two separate power supplies: the main power supply (VDD, contact 28) for digital parts including I/O and either the backup supply (VDD_B, contact #14) for non-volatile RTC&SRAM block in IT300/500 (VDD_BACKUP) ***or*** the low ripple analog supply for RF block in IT03-S (VDDRF). Note that the power supply nets inside of the IT MP modules utilize low ESR capacitors and therefore the external LDOs must be compatible with low ESR capacitor at output.

The connectivity is selected so that the VDDRF and VDD_BACKUP share the common input (VDD_B, contact 14) and the user must select either a regulator output for IT03-S or a battery backup (or super capacitor) supply for IT300/500.

Suggested IT MP supply voltage is +3.0… 3.3V for both supply inputs. With IT300/500 the VDD supply can be switched off when the navigation is not needed but keep the non-volatile VDD_B supply active all the time.

With IT03-S the both supplies should be activated at the same time within a few milliseconds. With IT03-S the low quiescent sleep state can be controlled by a serial command or by the On/Off control signal J4.

When the VDD supply is powered off with IT300/500, all the I/O should be also at low state or disconnected from the device. Pay attention especially to the RESET, BOOT and UART RX input signals, which are normally at high state.

NOTE

Since the antenna bias is generated internally from either VDD or from VDD_B supply, it is required that the VDD and VDD_B supply current is limited externally to 150mA max for short circuit protection. Note that IT500 has an internal current limit function and short circuit protection.

NOTE

Power supply inputs contain internal low ESR (abt. 0.01 ohm) decoupling capacitors. Make sure that the external power supply output for IT MP module is compatible with low ESR output capacitors.

4.4 Reset

The reset input XRESET (contact 9) is an active low asynchronous reset. The processor boots after the low-to-high transition. The XRESET input contains an internal voltage detector to force reset when VDD supply is below the specified range. For normal operation the XRESET input can be left unconnected.

4.5 UART

All receivers support UART communication via two serial ports: Port 0 and Port 1 (or Port A and B in IT300, respectively). Check details for default protocol settings and data speeds from respective technical documentation (*ref 1, 2, 3*). The configuration can be set by the user so that e.g. a common NMEA port and data speed is possible between IT MP receivers. Proprietary binary protocols are available for IT03-S (iTalk) and IT300 (SiRF binary).

I/O levels form the serial ports are CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed.

4.6 Boot Select

The boot source is defined in the internal boot ROM sector by using two BOOT1 and BOOT2 control inputs (pin 2 and 10, respectively), see table 2 for signal names with each module. After power up or after system reset these signal

states are read and the boot is processed according to the following table. The BOOT2 is reserved production and it should be left floating.

Table 3 Boot select

BOOT1 contact #2	IT300	IT03-S
high	Normal operation	Normal operation
low	UART Port A boot (Firmware update)	UART Port 0 boot (Firmware update)

After power up the BOOT1 signal should keep the intended state at least 500 ms.

In Normal mode the BOOT1 signal should keep the intended state at least 30us after XRESET low-to-high transition.

The standard firmware supports only the boot from internal Flash memory (normal operation) or boot from UART Port 0 (A).

NOTE

To ensure normal operation during system reset and power on, the BOOT1 input (contact #2) requires an external pull-up resistor connected to VDD. The pull-up resistor can be e.g. 4.7 kOhm.

Do not connect the BOOT2 signal (contact #10), it should be left floating. IT03-S has an internal pull-up resistor for proper BOOT2 configuration and the usage is reserved for production. With IT300 the BOOT2 signal is not used (no connection). With IT500 there is no HW-boot mode and therefore BOOT pins are not available.

4.7 Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides

also a bias supply, which is the same level as the VDD_B supply with IT03-S. With IT300/IT500 the antenna bias is generated internally from the VDD supply. During idle or sleep state the antenna bias is switched off.

The maximum tolerated antenna bias current for IT03-S is 100mA, which is current limited only by the external regulator supplying VDD_B. It is required that the VDD_B supply current is limited externally to 150 mA max.

With IT300 the antenna bias is current limited only by the external regulator supplying VDD. It is required that the VDD supply current is limited externally to 150 mA max.

The IT500 has an internal current limit function for the antenna bias. The maximum normal operation current for the antenna bias with the IT500 is 30mA while the internal current limit is set to 40mA. When a short circuit is present at the antenna pin, the current limit function will set the maximum short circuit current to 30mA.

NOTE

Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

4.7.1 Active GPS antenna

The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range from +6 dB to +32 dB.

4.8 PPS output

The PPS output provides a pulse-per-second signal, which can be used for timing purposes. For details see *ref 1,2 and 3*.

4.9 UART inputs

If either of the UART ports is not used, pull the RX signal to high state with a pull up resistor.

4.10 Dedicated HW control signals with IT300

4.10.1 ON_OFF input

The IT300 can be controlled to wake up from Push-to-Fix CPU only state by the ON_OFF control input (contact 1). The wake up interrupt is generated by a low-to-high toggle, which should be longer than 62us.

NOTE

If not used, pull ON_OFF signal to low state.

4.10.2 Backup state and I/O

During Backup state the processor is powered off and thus all inputs should be disconnected or set to low state, otherwise leakage current may flow due to internal I/O protection.

4.11 Dedicated GPIO with IT500

4.11.1 Valid fix indicator

The pin #12 can be used as a valid fix indicator output, which is at high state during signal acquisition and toggling with 50% duty cycle and 2s period when valid fix is available (see figure below).

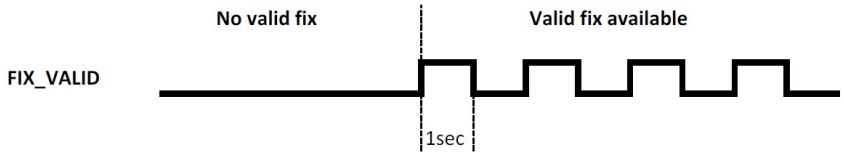


Figure 1. FIX_VALID output operation.

4.11.2 Antenna detector outputs

There are two antenna status pins in IT500. The functionality of these pins with different antenna status conditions is shown in table 4 below.

Table 1. Active antenna status output signals.

GPIO	Active Antenna OK	Antenna short	Antenna open or passive antenna
ANT_OK	High	Low	Low
XANTSHORT	High	Low	High

4.11.3 STANDBY control input

The Standby mode of the IT500 is initiated by falling edge at STANDBY pin. The module can be wake up from Standby mode by rising edge at the STANDBY pin. Note that when Standby function is not used, the STANDBY pin should be left not connected (nc). For more detailed information see ref. 2.

4.12 Dedicated GPIO with IT03-S

4.12.1 UI Indicators

With the standard IT03-S firmware there are three GPIO outputs dedicated as a driver for User Interface (UI) Indicators. These outputs can be used e.g. to drive LEDS, which gives information on the state of the receiver. For details see *ref 3*.

4.12.2 On/Off control input

With the standard firmware the IT03-S can be controlled to Sleep mode by the On/Off control input (SPI1SDO / GPIOB14, contact J4) or by a specific serial command. During Sleep Mode only the real time clock is running and the current consumption is reduced to about 20 uA.

Note that the worst case delay from the On/Off Control high-to-low transition to achieve Sleep mode and reduced current drain is 300 ms. The standard firmware stores the last known good position (LKG) and any Log data to the internal Flash memory before entering the Sleep mode.

Table 4 IT03-S On/Off control

On/Off Control contact #4	I/O	Signal description
High	I	Normal (navigating) mode, delay from Sleep mode 3 ms
Low	I	Sleep mode, delay from Normal mode 300 ms max.

NOTE

With the standard firmware the On/Off control input has an internal pull-up resistor 100kohm connected to VDDDIG and the signal can be left unconnected for normal operation. Note also chapter Sleep mode &I/O.

4.12.3 Wake Up control input

With the standard firmware the IT03-S can be waked up from sleep state by the Wake Up control input (SPI1SDI / GPIOB15, contact 6). Wake Up input is normally used only when the module has entered sleep state using the specific serial command.

Wake up interrupt is generated by toggling the Wake Up control input; in case of a pulse the pulse length should be at least 20 ms.

Table 5 Wake Up control

Wake Up Control contact #6	I/O	Signal description
High to Low	I	Wake up from sleep state, Low state at least 20ms
Low to High	I	Wake up from sleep state, High state at least 20ms

NOTE

With the standard firmware the Wake Up control input has an internal keeper circuit and the signal can be left unconnected for normal operation. Note also chapter Sleep mode &I/O.

4.12.4 Sleep mode and I/O

During Sleep mode in IT03-S all the dedicated GPIO are configured to inputs with internal 100kohm pull-down resistors. There is one exception: the On/Off control input is configured to 100k pull up resistor in case the sleep state is entered via a proper command to any of the serial Ports.

4.13 Mechanical dimensions and contact numbering

Module size is 16.2mm (typical) x 18.8mm (typical) x 2.5mm (max.). General tolerance is ±0.2mm.

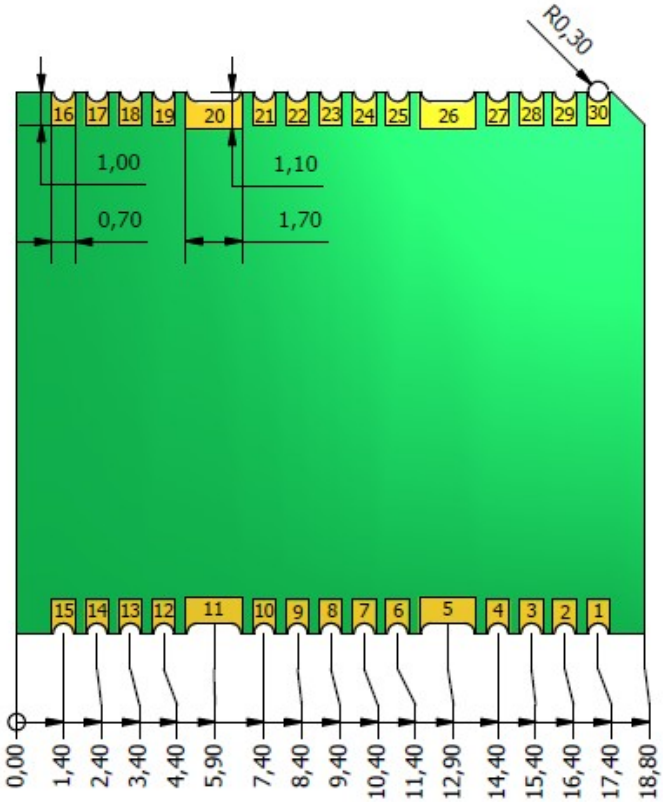


Figure 2. Contact numbering, bottom view.

Figure 1 Contact numbering, top view.

4.14 Suggested pad layout

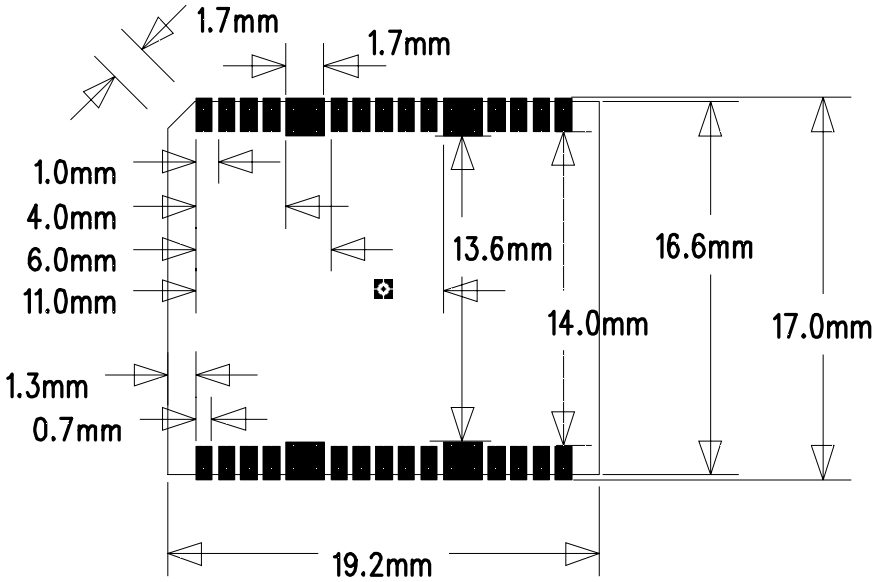


Figure 3. Suggested pad layout and occupied area, top view.

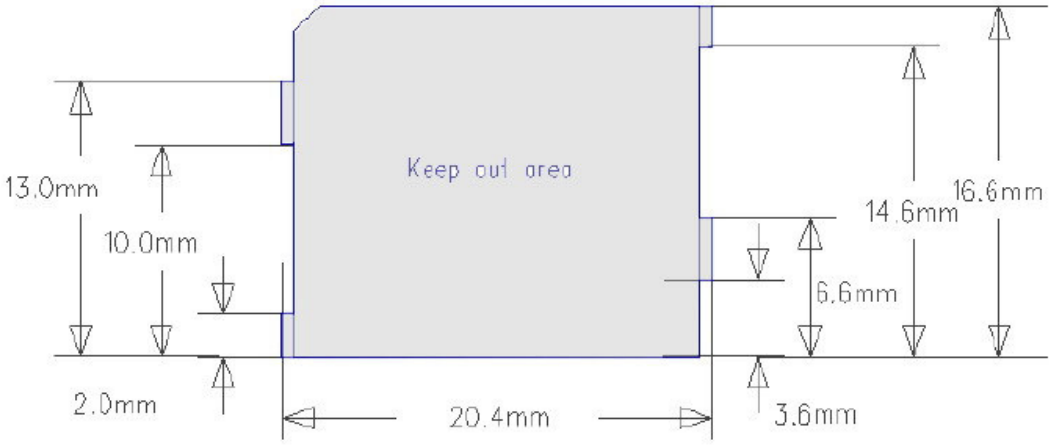


Figure 4. Suggested component keep out area, top view.

5. MANUFACTURING

5.1 Assembly

The IT MP modules support only assembly and soldering in a reflow process on the top side of the PCB. Also a lead free soldering profile is accepted. Read ref 4 for more information on reflow process for IT MP modules.

5.2 Moisture sensitivity

Note that the IT MP series modules are moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The modules must be stored in the original moisture barrier bag or if the bag is opened, the modules must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

6. REFERENCE DESIGN

The idea of the Multiplatform reference design is to give a guideline for the applications using the IT MP receivers. It highlights suitable external connectivity in order to achieve functional compatibility between IT MP receivers.

In the following two chapters the reader is also exposed to design rules that he should follow, when implementing IT MP receivers in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by surroundings. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

6.1 Simple Application Circuit Diagram

The Simple Application circuit (figure below) supports communication through the UART Port 0 (NMEA or binary protocols). Other required signals are the antenna input, supply voltage input (V_INPUT) and required external pull-up resistor (R2) for BOOT1 signal. External host control for XRESET and BOOT1 signals are suggested for firmware update via Port 0 (A) in HW-boot mode.

The circuit assumes that the V_INPUT supply voltage is active all the time. Suggested supply voltage for both VDD and VDD_B is +3.0V. The circuit supports also optionally the usage of external back up battery supply via diode D2 for IT300/500 using proper selection of jumper resistors.

Usually the user wants to power off the GPS when the navigation is not needed. For this purpose the IT MP supports an external control signal PWR_ON from host, which either controls the digital supply VDD (with IT300/500) or the J4 signal (On/Off control input with IT03-S) using proper selection of jumper resistors.

When the digital supply VDD is powered off with IT300/500, the backup supply VDD_B is active either via U2 or via external battery backup supply via D2. In this state, all the I/O should be also at low state or disconnected from the device. Pay attention especially to the RESET, BOOT and UART RX input signals, which are normally at high state. With IT03-S both regulated supplies VDD (U3) and VDD_B (U2) are active all the time.

The suggested regulator AAT3221IGV-3.0 from Analogic Tech is used for analog supply VDD_B due to the low quiescent current (1.1uA typ.), other types are suited as well, like Seiko S-1167B30. For digital supply VDD regulators with

faster load transient response are suggested, like Seiko S-1132B30 or National LP2985.

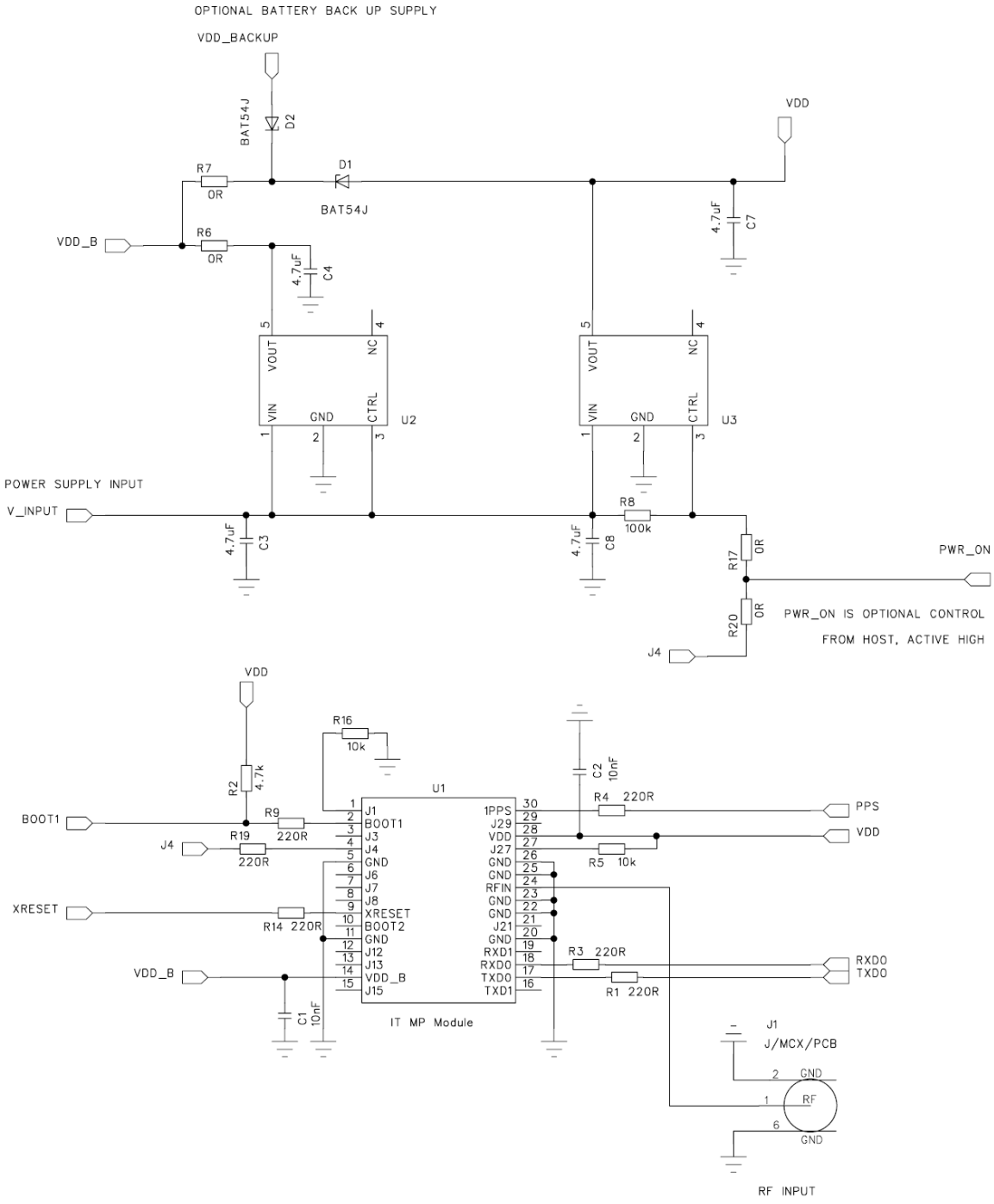


Figure 5. IT MP Simple Application Circuit Diagram.

Table 6 Simple Application Circuit: component usage

Component	IT500	IT300	IT03-S	Note
R2	-	4.7k	4.7k	BOOT1 pull up required
R6	0R	0R	0R	
R7	-	-	-	
U2	S-1167B30	S-1167B30	S-1167B30	VDDRF, low ripple
C3/4/7/8	4.7uF X5R 0805	4.7uF X5R 0805	4.7uF X5R 0805	
U3	S-1132B30	S-1132B30	S-1132B30	Digital supply
R17	-	-	-	No host control for PWR_ON
R20	-	-	-	No host control for PWR_ON
R8	100k	100k	100k	No host control for PWR_ON
D1/D2	-	-	-	No battery backup
R5/16	-	10k	-	Pull up/down for IT300
Usage of host control for PWR_ON:				PWR_ON control, active high
R8	-	-	100k	
R17	0R	0R	-	
R20	-	-	0R	
Usage of the battery back up supply:				
U2	-	-	AAT3221IGV-3.0	
C3/4	-	-	4.7uF X5R 0805	
D1/D2	BAT54J	BAT54J	-	
R6	-	-	0R	
R7	0R	0R	-	

6.2 General Application Circuit Diagram

The General Application circuit (figure below) is more general than the previous Simple Application Circuit. It supports also communication through the UART Port 0 (NMEA or binary protocols). Other required signals are the antenna input, supply voltage input (V_INPUT) and required external pull-up resistor (R2) for BOOT1 signal. External host control for XRESET and BOOT1 signals are suggested for firmware update via Port 0 (A) in HW-boot mode.

The circuit supports optionally two control signals from external host: a) a signal named PWR_ON, which can be used to control the low quiescent Sleep modes and b) wakeup interrupt signal using J1/J6 signals, which can be used to wake up the module from sleep state, which is useful especially when a special serial command is used to enter the sleep mode.

With IT03-S the low drop-out linear regulator U2 supplies +3.0V voltage to the RF and analog parts (VDD_B). The linearly regulated power supply is needed for VDD_B with IT03-S, because the maximum allowed ripple voltage for VDD_B is

2 mV(RMS). The digital supply (VDD) is taken either directly from the main +3.3V supply or from the regulator U3. With IT03-S the both supplies are kept active all the time.

With IT300 the VDD supply can be taken via a controlled regulator U3 (in this case +3.0V), which allows the host to control the VDD supply. When the VDD supply is powered off with IT300/500, all the I/O should be also at low state or disconnected from the device. Pay attention especially to the RESET, BOOT and UART RX input signals, which are normally at high state.

The U3 regulator can be optionally replaced with either the switch Q1 or with the jumper resistor R12, depending on usage of the low quiescent Backup state and if a suitable V_INPUT regulated supply voltage +3.0…+3.3V is available.

The regulator U2 is omitted by proper selection of the 0 ohm jumper resistors in case for the backup supply for IT300/500. The backup supply capacitor C9 can be omitted and replaced with D2 if a suitable battery backup supply voltage is already available. Also a re-chargeable Lithium battery can be used for back up supply instead of C9.

All the I/O signals are routed away from the module through series resistors. In this way the local oscillator (LO) signal leakage that is present at the I/O contacts is suppressed. Although the LO leakage is very small at the IO contacts of the module, it may still interfere the GPS reception, especially when the antenna is located very near to these signal routes.

For the same reason supply decoupling capacitors C1 and C2 should be connected very close to the module's with shortest possible traces to supply contacts and to ground plane.

Additionally, there must be another capacitor (4.7uF or bigger) from VDD to the ground. This capacitor can be located further away. If some specific signal is not needed, it contact can be left open by default.

Note that there is a DC voltage present at the RF input, when the module is operating in Normal mode. If a passive antenna with a short-circuit to the GND is used, an external series DC block capacitor (18pF) must be used for the RFIN signal line.

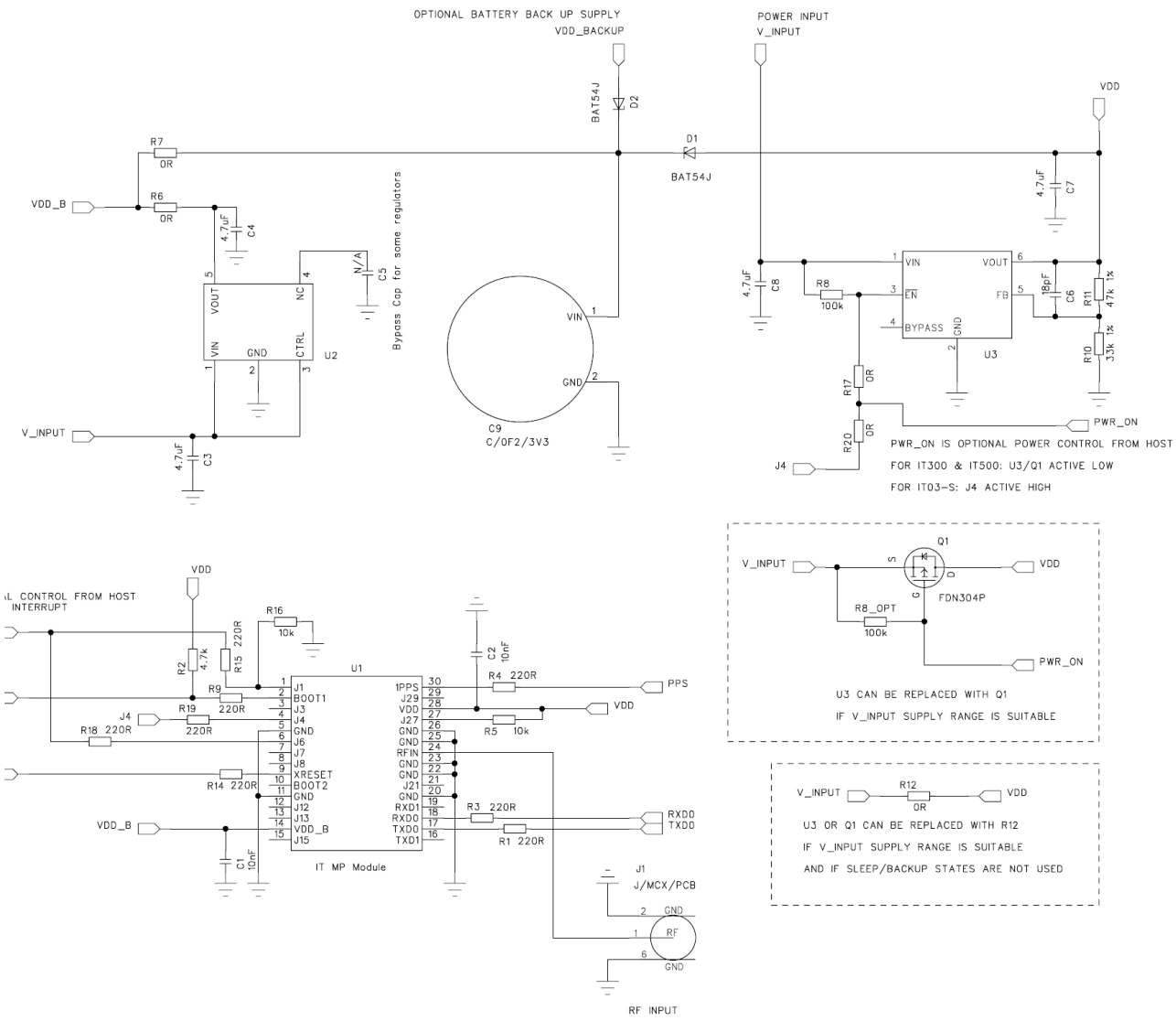


Figure 6. IT MP Application Circuit Diagram.

Table 7 Application Circuit: component usage

Component	IT500	IT300	IT03-S	Note
R2	-	4.7k	4.7k	BOOT1 pull up required
U2	-	-	S-1167B30	VDDRF, low ripple
C3 & C4	-	-	4.7uF	
C9	0.2F	0.2F	-	Also suitable >0.2F or re-chargable Lithium battery
R5	-	10k	10k	
R6	-	-	0R	
R7	0R	0R	-	
U3	TPS79101	TPS79101	S-1132B30	When V_INPUT > +3.3V
R10	33k 1%	33k 1%	-	With TPS79101
R11	47k 1%	47k 1%	-	With TPS79101
C6	18pF	18pF	-	With TPS79101
Q1	-	-	-	When V_INPUT +3.0... +3.3V
R12	-	-	-	When V_INPUT +3.0... +3.3V
R17	-	-	-	No host control for PWR_ON
R20	-	-	-	No host control for PWR_ON
R15	-	-	-	No host control for wake up
R16	-	10k	-	No host control for wake up
R19	-			No host control for wake up
Options:				
U3/Q1/R12	Q1 (FDN304P)	Q1 (FDN304P)	R12 (0R)	V_INPUT = +3.0...+3.3V, host control for PWR_ON
U3/Q1/R12	R12 (0R)	R12 (0R)	R12 (0R)	V_INPUT = +3.0...+3.3V, no host control for PWR_ON
R17	0R	0R	-	IT300 & IT500 host control for PWR_ON, active low
R20	-	-	0R	IT03-S host control for PWR_ON, active high
C9/D2	D2 (BAT54J)	D2 (BAT54J)	-	External battery back up supply
Usage of host wake up control:				
R15	-	0R	-	If host control for wake up, IT300
R18	-	-	0R	If host control for wake up, IT03-S

6.3 PCB layout issues

The suggested 4-layer PCB build up for IT MP receivers is presented in the following table.

Table 8 Suggested PCB build up

Layer	Description
1	Signal + Ground with copper keep-out below IT MP
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for the via holes, which can be placed close to the pad under the module. If possible, the amount of any VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT MP is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed very near to any of the IT MP modules. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C1 and C2 should be connected very close to the module's with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT MP to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes per GND pad.

The RF input should be routed clearly away from other signals. This minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board area free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers. For the 50 ohm RF input line use a wide gap (about 1.5x substrate thickness)

between the RF signal trace and the GND plane in order to sustain the right geometry for correct line impedance.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing symmetrical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

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