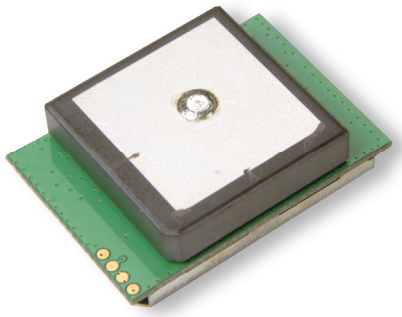

REV 1.2

Technical Description

Fastrax UP300 GPS Receiver

This document describes the electrical connectivity and main functionality of the Fastrax UP300 module.

September 1, 2009

Fastrax Ltd.

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Fastrax

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CHANGE LOG

Rev.	Notes	Date
0.1	First Draft	2006-10-13
0.2	Minor updates	2006-12-08
0.3	Updated specs, minor updates	2007-01-15
0.4	Minor corrections	2007-02-05
1.0	Added chapter 3. Operation. Updated antenna bias threshold to 3mA. Height updated to 7.2mm	2007-03-30
1.1	Updated mechanical drawing	2007-04-25
1.2	Major update to HW revision C (update to GSC3f/LPx)	2009-09-01

CONTENTS

COMPLEMENTARY READING

The following SiRF reference documents are also complementary reading for this document.

Ref. #	File name	Document name
I	GSC3LPxProductInsert.pdf	GSC3e(f)/LPx Product Insert
II	NMEA Reference Manual.pdf	NMEA Reference Manual
III	SiRF Binary Protocol Reference Manual.pdf	SiRF Binary Protocol Reference Manual
IV	APNT3008.pdf	SiRF Application Note Power Management Considerations of SiRFstarIII

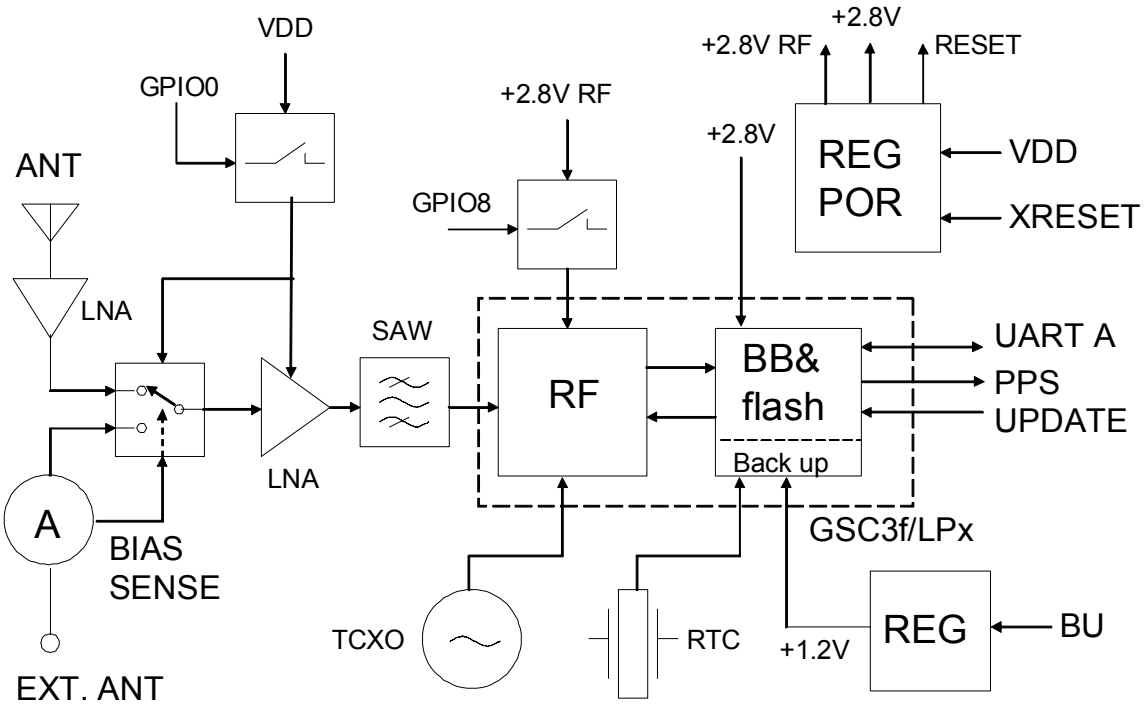
1 GENERAL DESCRIPTION

The UP300 is an OEM GPS receiver module, which uses the SiRF single chip receiver GSC3e/LPx *(ref 1)* with tiny form factor 19.0 x 27.0mm. The UP300 receiver provides very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations. The module operates with the SiRF firmware GSW3 from an internal 4 Mbit flash memory.

The module provides complete signal processing from internal antenna to serial data output in NMEA (or SiRF binary) messages. The module requires a power supply VDD and a back up supply voltage BU for non-volatile RTC & RAM blocks. The UP300 module interfaces to the customer's application via one serial port, two control signals and PPS timing signal. Serial data and all I/O signal levels are CMOS compatible.

The antenna input connector supports external active antenna connectivity. Switching from embedded patch antenna to an external antenna is handled automatically. UP300 provides also internally generated antenna bias supply at the external antenna connector.

1.1 Block diagram



1.2 Frequency Plan

Clock frequencies generated internally at the UP300 receiver:

- 32768 Hz real time clock (RTC)

- 16.369 MHz master clock (TCXO)
- 1571.424 MHz local oscillator of the RF down-converter

2 SPECIFICATIONS

2.1 General

Table 1 General specifications

Receiver	GPS L1 C/A-code, SPS
Channels	20 physical (limited to 12 tracking by firmware)
Update rate	1 Hz default (fix rate configurable)
Acquisition Sensitivity (Cold)	-146dBm typ. (note 1)
Tracking Sensitivity	-159dBm typ. (note 1)
Supply voltage, VDD	+3.0V…+3.6 V
Back up supply voltage, BU	+1.5V…+3.6 V (preferably active all the time)
Power consumption, VDD	81 mW typical @ 3.0V (without Antenna bias)
Power consumption, BU	18 uW typical @ 3.0V (during battery backup state)
External antenna net gain range	+10…+30 dB
External antenna bias voltage	VDD (+/- 0.0V… -0.2V)
External antenna bias current	>1.5mA (typ.), limited to max 50mA (typ.)
Operating temperature range	-30ºC…+85ºC (note 2)
Serial port protocol	Port A: NMEA (switchable to SiRF binary)
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	NMEA: 9600 baud
PPS output	+/- 1us accuracy
I/O signal levels	TXA, RXA, UPDATE & PPS: 2.8V CMOS compatible: low state 0…0.8V; high state 2.0…2.8V. Inputs are 3.3V tolerable. XRESET: 1.2V CMOS compatible: low state 0…0.3V; high state 0.9… 1.2V. Input is 3.3V tolerable.
I/O sink/source capability	+/- 2 mA max.
I/O connector type, mating part	JST 08SUR-32S
External Antenna connector, mating part	Hirose e.g. U.FL-LP-066

Note 1: Measured at antenna connector and with an external LNA NF=1.5dB.

Note 2: Usage in the temperature range –40°C… –30°C is accepted but Time-to-First-Fix may be increased.

2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	500	mW
Supply voltage, VDD	-0.3	+5.0	V
Supply voltage, BU	-0.3	+5.5	V
Current output on antenna input	0	+150	mA
Input voltage on any input connection	-0.3	+3.6V	V
RF input level	-	+15	dBm

3 OPERATION

3.1 Operating modes

After power up UP300 boots from the internal flash memory for normal operation. Modes of operation:

- Navigating mode
    - Back up state
    - Power management system mode (TricklePower)
- Programming mode

3.2 Normal mode

The UP300 receiver enters navigating mode after power up. It will start navigation automatically after power up/reset using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM). The power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as Full-power state.

Navigation is available as long as the VDD and BU power supplies are active. Navigation can be stopped by switching VDD off by the host while keeping BU active, which is called also as *Back up* state.

Any configuration settings are valid as long as the back up supply BU is active. When the BU is powered off, the configuration is reset to factory configuration on next power up.

3.2.1 Firmware configuration

Fastrax default SiRF GSW3 firmware configuration *(ref III)*, firmware variant ***CAR***:

1. Port A: NMEA 9600 baud
2. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
3. Port B: no protocol
4. Track smoothing: disabled
5. Static navigation: enabled
6. DGPS/SBAS: disabled
7. Datum: WGS84

3.3 Back up state

Back up mode means a low quiescent power state where only the internal non-volatile RTC and RAM block is powered on via BU supply. The main supply input VDD is powered off and navigation is halted.

When the main supply VDD is powered on again, the receiver will start navigation automatically with fastest possible TTFF using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM).

3.4 Power management modes

The receiver supports also SiRF operating modes for reduced average power consumption (*ref IV*) like Adaptive TricklePower mode *(Push-to-Fix* mode is not supported due to lack of ON_OFF control input):

1. *Adaptive TricklePower:* In this mode the receiver stays at Full Power for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in a low power Stand-by state to reduce current drain down to 0.7mA (typ.). TricklePower mode is configurable with SiRF binary protocol message ID151 (*ref III*). The receiver stays once in while in Full Power automatically to collect new ephemeris and almanac data from rising satellites.

Note that position accuracy is somewhat degraded in power management mode when compared to full power operation.

3.5 Programming mode

Re-programming via HW-booting mode is utilized by keeping the UPDATE control input at low state during power up or at system reset. Now the GPS module boots from the serial data Port A and waits for the boot loader commands from the host (an application running on the host, SIRFFlash). It is suggested that all applications should support the HW-booting by access to serial Port A (TX & RX), UPDATE and XRESET signals.

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to the host without any transferring utilities that may cause a failure during speed change.

3.6 Procedure for re-programming the firmware

1. Connect serial Port A to PC.
2. Set the module to UART boot mode: Power up the module with UPDATE signal low. Alternatively give a XRESET pulse while keeping UPDATE signal low after the power supply is on.
3. Start SiRFFlash application on PC.
4. Browse for the flash *.s file.

5. Check the Communication setting from the SiRFFlash to meet your PC serial port.

6. Press Execute at SiRFFlash. Now the flashing starts.

7. After flashing has finished, boot the receiver normally with UPDATE signal high either by cycling the power supply or by giving a XRESET pulse high-low-high.

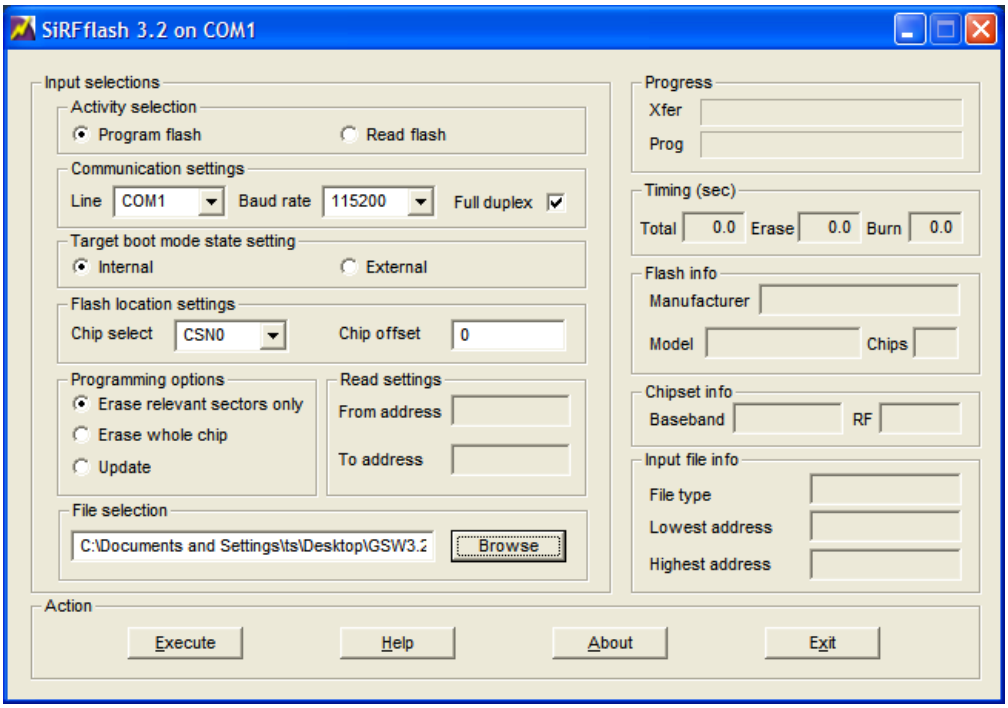


Figure 1 SiRFFlash default settings.

4 CONNECTIVITY

4.1 Connection assignments

The I/O connections are available on the 8-pin interface connector. The connector is from JST, type SM08B-SURS-TF. Mating connector is e.g. JST 08SUR-32S.

Table 3 Connections

Contact	Signal name	I/O	Alternative signal name	Signal description
1	TXA	O	-	UART Port A async. Output
2	RXA	I	-	UART Port A async. Input. Pulled high internally with 100k resistor.
3	GND	-	-	Ground
4	VDD	I	-	Main power supply
5	BU	I	-	Backup supply
6	XRESET	I	-	Asynchronous system reset, active when low. Pulled high internally with 100k resistor.
7	UPDATE	I	-	Boot control input 1: 0=UART, 1=Internal flash memory. Pulled high internally with 10k resistor.
8	1PPS	O	GPIO9	1PPS signal output

4.2 Power supply

The UP300 module requires two separate power supplies: BU for non-volatile back up block (RTC/RAM) and the VDD for digital parts and I/O. RF and digital sections have internally regulated +2.8V supplies. VDD can be switched off when navigation is not needed but if possible keep the back up supply BU active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Back up supply BU draws typically 6uA current in back up state. During navigation BU current may peak up to 70uA typ.

Main power supply VDD current varies according to the processor load and satellite acquisition. Typical VDD peak current is 35mA during acquisition after power up without external antenna bias current.

Both power inputs have internal ceramic, low ESR capacitors. Use a power supply or regulator that is compatible with low ESR (~ 0.01 ohm) ceramic output load capacitors.

NOTE

Use a power supply or regulator that is compatible with low ESR (~ 0.01 ohm) ceramic output load capacitors.

4.3 Reset

The reset input XRESET is an active low asynchronous reset. The processor boots after the low-to-high transition depending on the state of the UPDATE signal. The XRESET input contains an internal voltage detector to force reset during power up or power down transitions.

The input has internal 100k pull up resistor to VDD. For normal operation the XRESET input can be left unconnected.

NOTE

XRESET input is CMOS 1.2V compatible. For proper reset pull input below 0.3V. The input is 3.3V tolerable and is pulled high with internal 100kohm resistor to VDD.

4.4 Boot Select

The boot source is defined in the internal boot ROM sector by using the UPDATE control input. After power up or after system reset the value is read and the boot is processed according the following table.

Table 4 Boot select

UPDATE	I/O	Boot source
high	I	Boot for internal flash memory (Normal operation)
low	I	External boot UART Port A for re-programming

UPDATE signal should be kept valid after power up for at least 500 ms to allow the internal power-on-reset delay to settle.

In Navigating mode the Boot Select should be kept valid for at least 10us after XRESET low-to-high transition.

4.5 Antenna input

The module provides embedded patch antenna as well as a connector for external active antenna. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides also a bias supply which is equal to VDD.

The module switches automatically between the internal and external antenna by sensing the external antenna bias current. When the bias current exceeds 1.5mA at the external antenna connector, the antenna signal is switched automatically from embedded antenna to the connector input.

The antenna bias current is limited by hardware to 50mA (typ.). In case there is a short circuit at the external antenna input the module will automatically switch back to embedded antenna. This state stays on until the short circuit is removed after which the antenna signal is switched back to external antenna connector in case there is proper antenna bias current present as described above.

The external antenna input connector is HIROSE UFL series. Mating connector is e.g. Hirose U.FL-LP-066.

4.6 UART

The device supports UART communication via Port A. With the default firmware the Port A is configured by default to NMEA protocol with 9600 baud and Port B to no protocol. The Port A is used also when the device is booting from the serial port.

The default configuration for Ports and respective protocols can be changed by commands via NMEA or SiRF binary protocols *(ref II & III)*. Any custom configuration settings stay active as long as the back up supply BU is active.

I/O levels form the serial ports are 2.8V CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed. Inputs are 3.3V tolerable.

4.7 PPS/GPIO9

The pulse-per-second (PPS) output provides an output for timing purposes. It shares the PPS functionality with GPIO9 for custom purposes.

4.8 Mechanical dimensions and contact numbering

Module size is 19.0mm (width) x 27.0mm (length) x 7.2mm. General tolerance is +/-0.3mm.

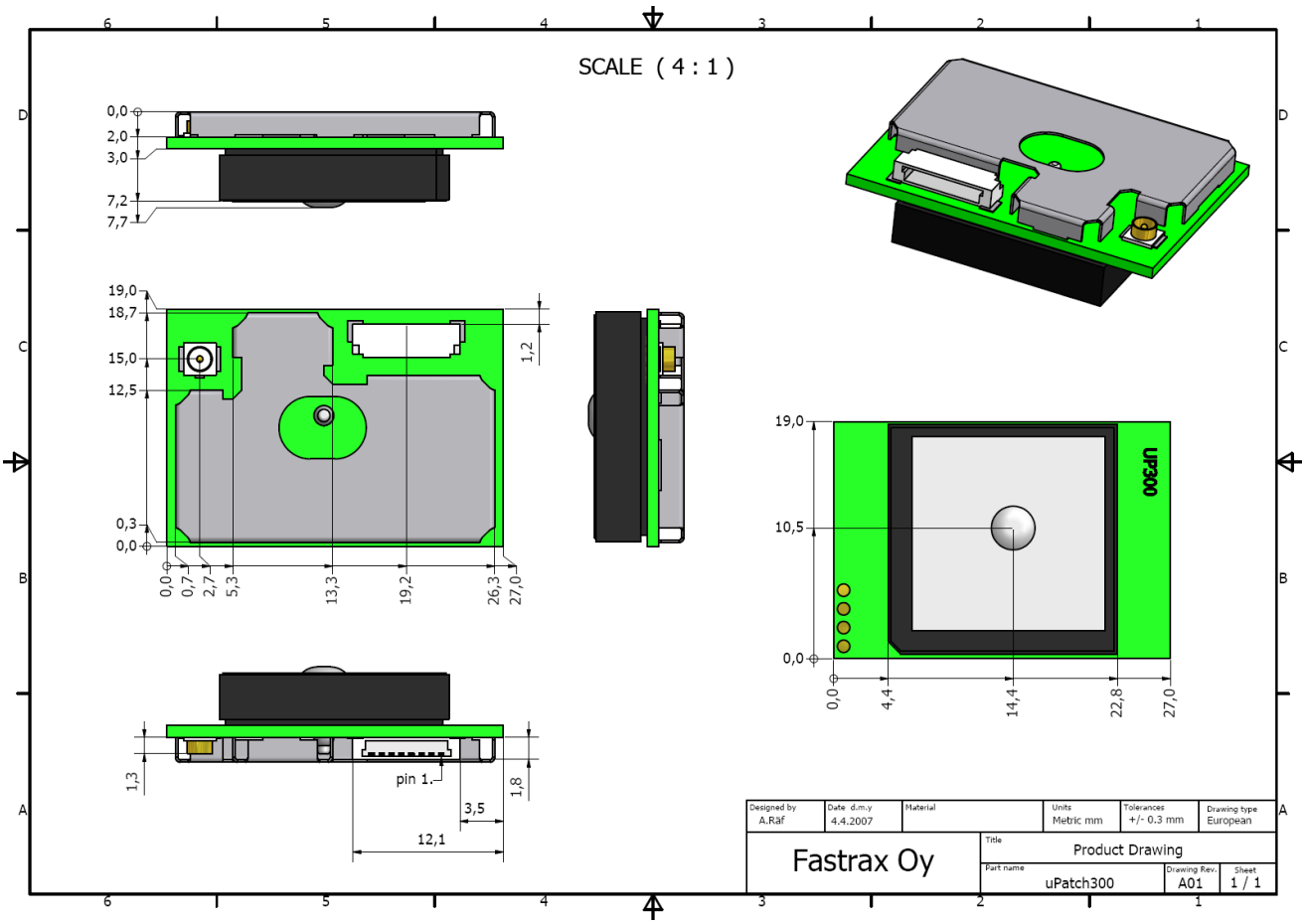


Figure 2 Mechanical outline.